I²S Digital Input, built-in one-wire pulse and level dual-mode channel selection, 3.1W Mono Class D Audio Power Amplifier

General Description

IU7191T is a high-efficiency, ultra-low electromagnetic interference (EMI) 3.1W mono Class-D audio power amplifier supporting I²S digital audio signal input. It integrates a digital-to-analog converter (DAC) and a multi-stage Class-D modulator internally, delivering excellent audio performance. Transmitting signals to the amplifier through the chip's I²S digital audio serial interface can significantly reduce the impact of noise sources on the transmitted audio, while avoiding the noise caused by the built-in audio decoding DAC of the main control chip, ultimately achieving a high signal-to-noise ratio and low total harmonic distortion. The closed-loop digital input design of IU7191T not only retains the advantages of digital amplifiers but also features outstanding PSRR and audio performance.

As a mono audio power amplifier, IU7191T supports three channel selections (left/right/mixed) through two methods: different level settings of the SD pin or one-wire pulse input. The chip also allows for flexible combination into stereo products by using two chips simultaneously. Additionally, IU7191T is equipped with built-in over-current protection, short-circuit protection, and thermal protection functions, effectively safeguarding the chip from damage under abnormal operating conditions. It offers a compact DFN2X2_10L package for customer selection, with a rated operating temperature range of -40°C to 85°C.

Features

- Output Power
  - P_O at THD+N=10% VDD = 5.0V
    - R_L=8Ω 1.8W(TYP)
    - R_L=4Ω 3.16W(TYP)
  - P_O at THD+N=1% VDD = 3.6V
    - R_L=8Ω 0.74W(TYP)
    - R_L=4Ω 1.3W(TYP)
- Operating Voltage Range: 2.5V to 5.5V
- Default I²S serial digital audio input interface
- Excellent Pop Noise Suppression
- Supports a Wide Range of Sampling Rates : 8KHz~196KHz
- Three channel options (left/right/mixed) are available, which can be set through two methods: SD pin level selection or one-key pulse input
- Class-D Structure without Filtering
- Up to 90% Efficiency
- High PSRR: -80dB at 217Hz
- Overcurrent Protection, Short Circuit Protection and Overheat Protection
- RoHS Compliant Lead Free Packaging

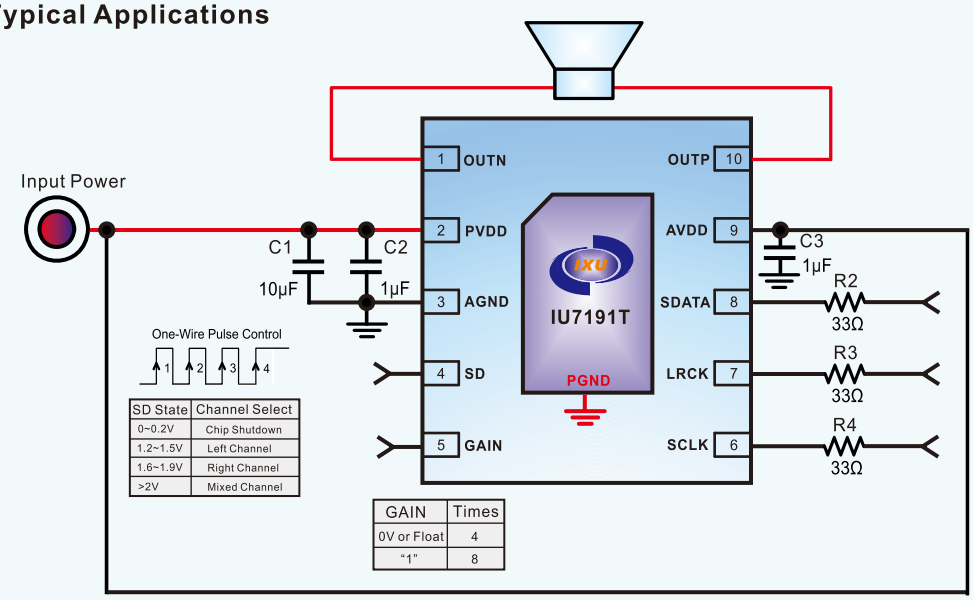
Applications

- USB Speaker/Portable Speaker
- PMP/MP4/MP5 Player
- GPS
- Digital Photo Frame

Package

- DFN2X2_10L

Typical Applications



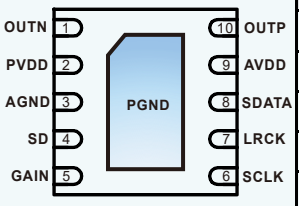
SD State	Channel Select
0~0.2V	Chip Shutdown
1.2~1.5V	Left Channel
1.6~1.9V	Right Channel
>2V	Mixed Channel

GAIN	Times
0V or Float	4
"1"	8

Notes:
(1) All chip capacitors should be arranged as close to the chip pin as possible.
(2) If the SD pin of the chip is used to select channels through level signals, it is recommended that the signal pass through an RC filter before entering the SD pin.
(3) The solid red line in the figure shows the path of high current flow.

PIN Configuration and Functions

DFN2X2_10L



(TOP PERSPECTIVE)



(TOP VIEW)

NO.	NAME	I/O	DESCRIPTION
1	OUTN	O	Audio output negative end
2	PVDD	P	Power input supply
3	AGND	-	Analog ground
4	SD	I	Left and right channel switching control and chip off control pin
5	GAIN	I	For the gain control pin, floating or grounding it provides a 4xgain while connecting it to a high-level input provides an 8xgain.
6	SCLK	I	I^2S bit clock pin
7	LRCK	I	I^2S Left and right channel frame clock pin
8	SDATA	I	I^2S Serial data input pin
9	OUTP	O	Audio output positive end
10	AVDD	P	Analog input supply
11	PGND	-	Power ground

Absolute Maximum Ratings [1]

SYMBOL	PARAMETER	VALUE	UNIT
VMAX	AVDD,PVDD,GAIN,SD,SDATA,LRCK,SCLK,OUTP,OUTN	-0.3~6	V
T_J	Junction operating temperature range	-40~150	℃
T_{STG}	Storage temperature range	-55~150	℃
T_{SDR}	Lead temperature (Soldering, 10 sec.)	260	℃

Recommended Operating Conditions

SYMBOL	PARAMETER	VALUE	UNIT
V_{IN}	Input power supply voltage	2.5~5.5	V
T_J	Junction operating temperature range	-40~125	℃
T_A	Ambient temperature range	-40~85	℃

Thermal Information [2]

SYMBOL	PARAMETER	VALUE	UNIT
θ_{JA}	Package thermal resistance - chip to environment thermal resistance	80	℃/W

Ordering Information

Product Name	Package Type	Device Marking	Reel Size	Tape width	Quantity
IU7191T	DFN2X2_10L	HBJB XXXX	7″	8mm	3000

ESD Range

HBM (Human Body Model) ---------- ±2kV

MM (Machine model) ---------- ±200V

1. The above parameters are only the limit values of device operation. It is not recommended that the working conditions of the device exceed the limit values. Otherwise, the reliability and life of the device will be affected, and even permanent damage will be caused.
2. Where the PCB board is placed in IU7191T, a heat dissipation design is needed. The heat sink at the bottom of IU7191T is connected with the heat sink area of PCB board.

Electrical Characteristics (Unless otherwise specified , T_A=25℃ , V_{DD}=5V , f_S=48KHz , default I^2S format)

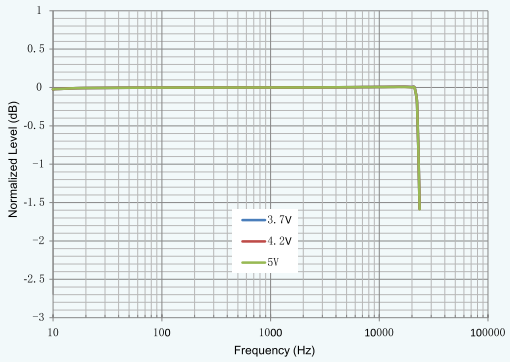
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		2.5		5. 5	V
I_Q	Power quiescent current	SCLK, LRCK have signals, SDATA=0 No Load		8.5		
		SCLK=LRCK=SDATA=0 No Load		3		
I_{SD}	Turn off leakage current	V_{SD} =0V		1		μA
V_{OS}	Output offset voltage			5	43	mV
PSRR	Power supply ripple rejection ratio	V_{DD}=2.5V~5.5V, 217Hz		-80		dB
CMRR	Common mode rejection ratio	VIN = 0V, V_{DD}=2.5V~5.5V		-70		dB
f_{SW}	Modulation frequency	V_{DD}=2.7V to 5.5V		400		KHz
η	Efficiency	P_O=0.6W, R_L=8Ω, V_{DD} =5V		87		%
V_{SD}	SD Voltage threshold	Left Channel	1.2		1.5	V
		Right Channel	0.6		1.2	
		Mixed Channel	2			
		Shut-down Low power shutdown	0		0.2	
T_{OFF}	SD Turn off time	V_{SD}=0V		25		us
T_{ST}	SD Start-up time			7		ms
V_{IH}	Input voltage high level	SCLK, LRCK, SDATA,GAIN	1.6			V
V_{IL}	Input voltage low level	SCLK, LRCK, SDATA,GAIN			0.2	V

Electrical Characteristics (Unless otherwise specified , T_A=25℃ , V_{DD}=5V , f_S=48KHz , default I^2S format)

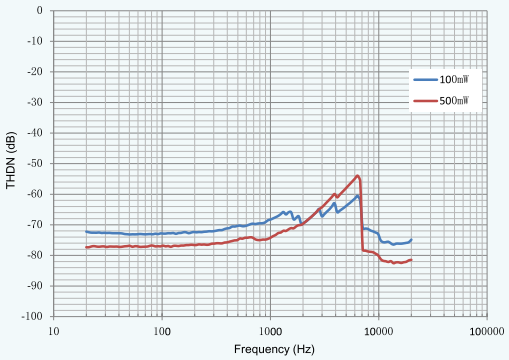
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	V_{DD}=5V, f=1KHz, R_L=4Ω, THD+N= 10%		3.16		W
		V_{DD}=5V, f=1KHz, R_L=4Ω, THD+N= 1%		2.50		
		V_{DD}=5V, f=1KHz, R_L=8Ω, THD+N= 10%		1.8		
		V_{DD}=5V, f=1KHz, R_L=8Ω, THD+N= 1%		1.40		
		V_{DD}=4.2V, f=1KHz, R_L=4Ω, THD+N= 10%		2.2		
		V_{DD}=4.2V, f=1KHz, R_L=4Ω, THD+N= 1%		1.8		
		V_{DD}=4.2V, f=1KHz, R_L=8Ω, THD+N= 10%		1.20		
		V_{DD}=4.2V, f=1KHz, R_L=8Ω, THD+N= 1%		1.00		
		V_{DD}=3.6, f=1KHz, R_L=4Ω, THD+N= 10%		1.59		
		V_{DD}=3.6V, f=1KHz, R_L=4Ω, THD+N= 1%		1.3		
		V_{DD}=3.6V, f=1KHz, R_L=8Ω, THD+N= 10%		0.92		
		V_{DD}=3.6V, f=1KHz, R_L=8Ω, THD+N= 1%		0.74		
THD+N	Total harmonic distortion+noise	V_{DD}=5V, P_O=0.6W, f=1KHz, R_L=8Ω		0.02		%
		V_{DD}=4.2V, P_O=0.4W, f=1KHz, R_L=8Ω		0.03		
		V_{DD}=3.6V, P_O=0.4W, f=1KHz, R_L=8Ω		0.028		
SNR	Signal to Noise Ratio	R_L=4Ω@1W 32 word Width 24 bit depth 48K sampling rate		90		dB

Typical Characteristics (Unless otherwise specified , T_A=25℃ , V_{DD}=5V , f_S=48KHz , default I^2S format)

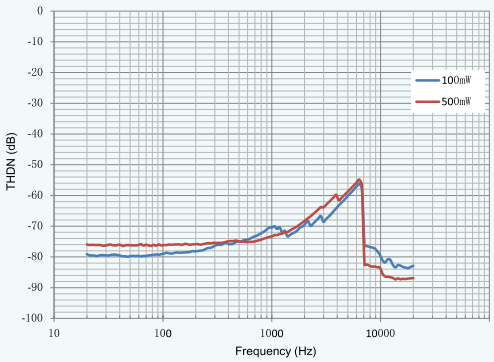
Normalised Frequency Response



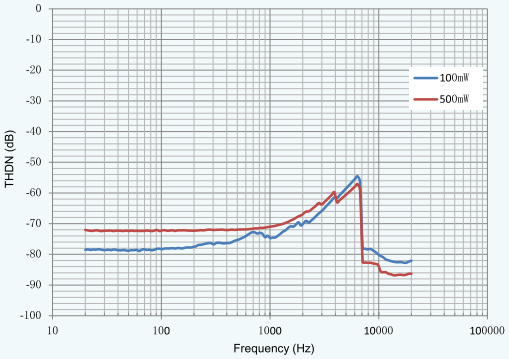
THD+N vs Frequency Vdd=5.0V Rl=4 Ohms



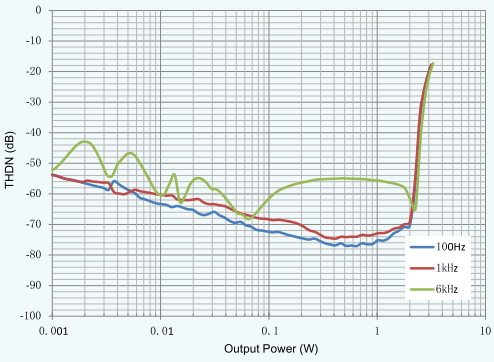
THD+N vs Frequency Vdd=5.0V Rl=8 Ohms



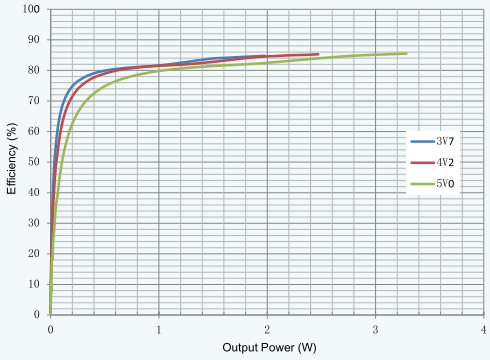
THD+N vs Frequency Vdd=3.7V Rl=8 Ohms



THD+N vs Output Power Vdd=5.0V Rl=4 Ohms



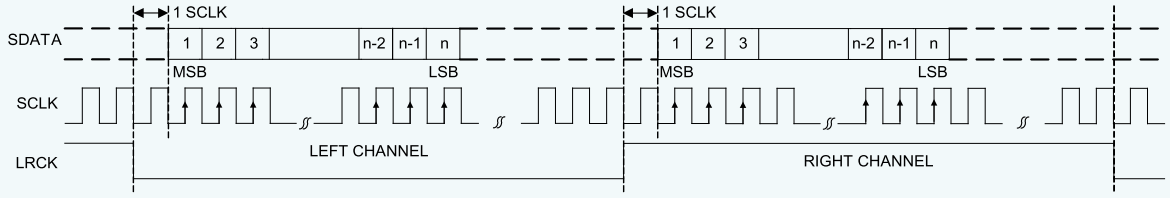
Efficiency vs Output Power Rl=4 Ohms



IU7191T Application Points

1. I²S Digital Audio Input

IU7191T can accept up to 24 bits of I²S serial audio input data. The standard I²S has three main signals: serial clock SCLK, frame clock LRCLK, and serial data SDATA. The I²S digital audio format is shown in the following figure:

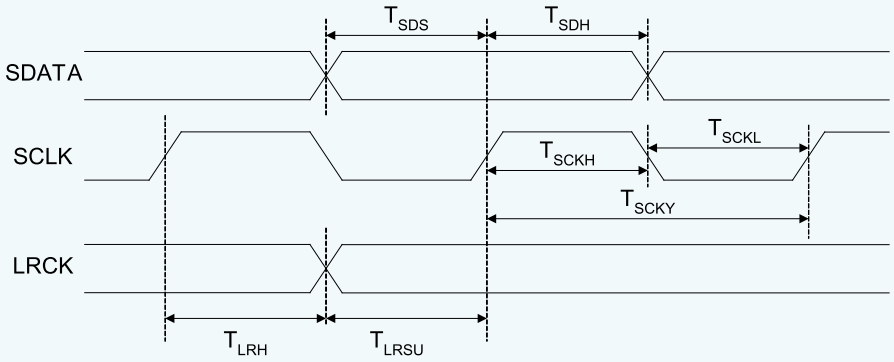


I²S serial audio data format up to 24-bit

Serial clock SCLK, also known as bit clock, refers to each bit of data corresponding to digital audio. The frame clock LRCK is used to switch data between left and right channels. A LRCK of "1" indicates that the data being transmitted is from the right channel, while a LRCK of "0" indicates that the data being transmitted is from the left channel. The frequency of LRCK is usually set to the audio signal sampling frequency.SDATA is serial data that is transmitted on a data line in the form of binary complement in I²S. Transfer the highest bit MSB first. Sending MSB first is because the word length of the sending and receiving devices may be different. When the system word length is longer than the data sending end word length, data transmission will experience truncation. That is, if the data receiving end receives data bits that are longer than its specified word length, all bits after the LSB with the lowest specified word length will be ignored. If the received word length is longer than its specified word length, the remaining bits will be filled with 0. In this way, the most significant bit of the audio signal can be transmitted, ensuring the best auditory effect.

2. Timing Specifications in I²S Digital Audio Format

IU7191T always serves as a slave, and attention should be paid to the margin of sending delay and receiving device establishment time. All timing requirements are related to the clock cycle or the minimum allowed clock cycle of the device. The signal wordwidth supports 8, 10, 12, 14, ..., 54, 56, 60, 64.



Serial Audio Port Timing

PARAMETER	SYMBOL	MIN	MAX	UNIT
LRCK Frequency		8	196	KHz
LRCK Duty Cycle		40	60	%
SCLK Frequency		0.128	13.824	MHz
SCLK Pulse Width Low	T_{SCKL}	15		ns
SCLK Pulse Width High	T_{SCKH}	15		ns
SCLK Rising to LRCK Edge Delay	T_{LRH}	10		ns
SCLK Rising to LRCK Edge Setup Time	T_{RSU}	10		ns
SDATA Valid to SCLK Rising Setup Time	T_{SDS}	10		ns
SCLK Rising to SDATA Hold Time	T_{SDH}	10		ns

Serial Audio Port Switching Characteristics

3. Left and Right Channel LRCK Settings

IU7191T is a single channel amplifier, while the standard I²S protocol can simultaneously transmit left and right channel signals. The chip selects left or right channel signals through the level setting of the SD pin. The frequency of LRCK is usually set to the audio signal sampling frequency, but different sampling frequencies support different SCLK frequencies.

4. Input Channel Selection Settings

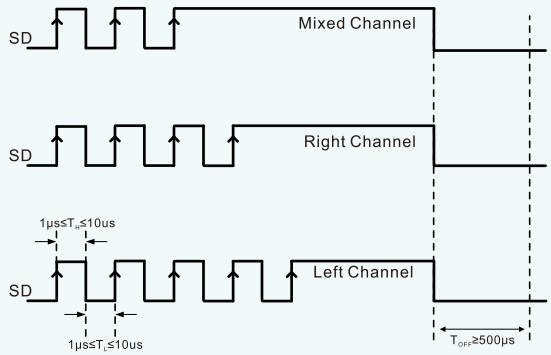
The IU7191T input channel is selected through the level setting of the SD pin. As shown in the table below:

SD State	Channel Select
0~0.2V	Chip Shutdown
1.2~1.5V	Left Channel
1.6~1.9V	Right Channel
>2V	Mixed Channel

Another way to select the input channel of the IU7191T is through the one-wire pulse method. The number of rising edges of the one-wire pulse signal determines the operating mode of the chip, as shown in the figure below.

When the SD pin receives a signal sequence of high→low→high→low→high (i.e., 3 rising edges), the chip selects the mixed channel. When the SD pin receives 4 rising edges, the chip selects the right channel. When the SD pin receives 5 rising edges, the chip selects the left channel. When rewriting the pulse to select a channel again, the SD pin must first be pulled low for more than 500μs to enter the shutdown mode before a new pulse can be written.

In the timing diagram of the one-wire pulse signal: T_H/T_L refers to the high/low level width of the pulse, respectively, and both are recommended to be 2μs; T_{OFF} refers to the low-level time required for the chip to enter the shutdown mode.



Timing diagram of one-wire pulse signal

5. No Filter Required

The IU7191T adopts a PWM modulation method that does not require a filter, eliminating the LC filter of traditional D-class amplifiers and improving efficiency, providing a smaller area and lower cost implementation solution for portable audio subsystems.

6. Pop & Click Suppression

IU7191T is equipped with a proprietary timing control circuit to achieve comprehensive Pop&Click suppression, effectively eliminating transient noise that may occur during power on, power off, shutdown, and Wake up operations.

7. Protection Circuit

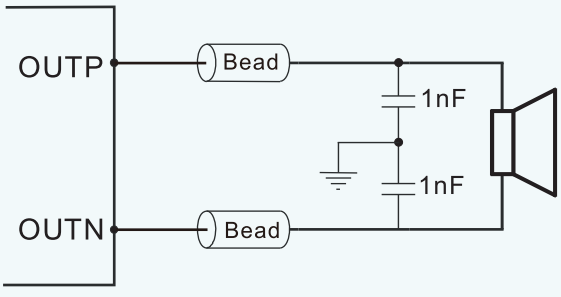
During the application process of IU7191T, when the chip experiences a short circuit between the output pin and the power or ground, or a short circuit fault between the outputs, the overcurrent protection circuit will turn off the chip to prevent damage. After the short circuit fault is eliminated, IU7191T automatically resumes operation. When the chip temperature is too high, the chip will also be turned off. After the temperature drops, IU7191T can continue to operate normally. When the power supply voltage is too low, the chip will also be turned off. After the power supply voltage is restored, the chip will start again.

8. Selection of Decoupling Capacitor

IU7189T is a high-performance Class D audio amplifier that requires an appropriate power supply decoupling capacitor to ensure high efficiency and optimal total harmonic distortion at the power supply end. At the same time, in order to achieve good high-frequency transient performance, it is hoped that the ESR value of the capacitor should be as small as possible. Generally, a capacitor with a typical value of 1uF is selected to bypass to ground. Decoupling capacitors should be placed as close to the VDD of the chip as possible in the layout, which is crucial for improving the efficiency of Class D amplifiers, as any resistance or self inductance between the device and capacitor can lead to a decrease in efficiency. If you want to better filter out low-frequency noise, you need to add a 10uF or larger decoupling capacitor according to the specific application.

9. Magnetic Beads and Capacitors

IU7189T can still meet the FCC standard requirements for a 60cm audio cable without magnetic beads and capacitors. When the output audio cable is too long or the device layout is close to EMI sensitive devices, it is recommended to use magnetic beads and capacitors. Magnetic beads and capacitors should be placed as close to the chip as possible.



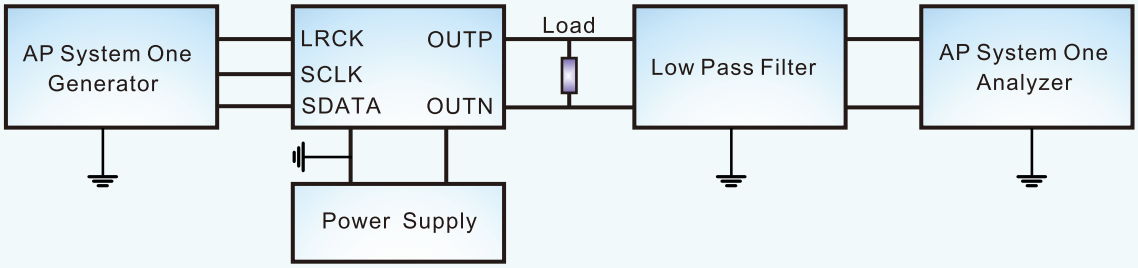
10. Gain Settings

The gain of the Class-D amplifier inside the IU7191T chip can be selected as 4 times or 8 times, which can be specifically set through the input of the chip's GAIN pin.

GAIN	Times
0V or Float	4
“1”	8

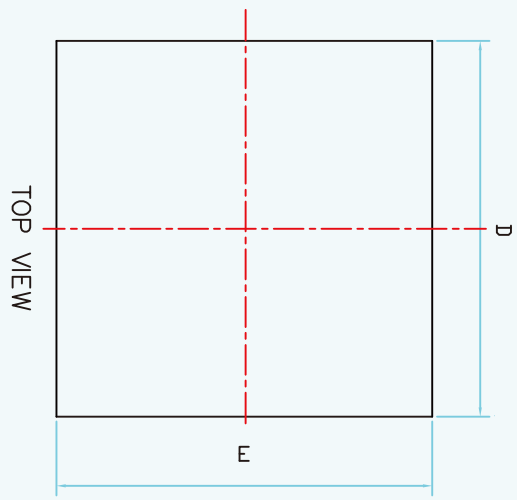
11.Test Circuit

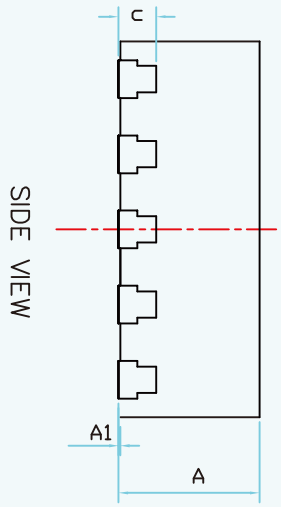
The IU7191T test circuit is shown below. When measuring a Class D mode power amplifier, a low-pass filter is necessary. Two 33uH inductors can be connected in series at both ends of the load resistor to equivalent a speaker. If only pure resistance is used to replace the speaker load, the measured results will be worse than when the speaker is loaded, including power, efficiency, distortion and other indicators.

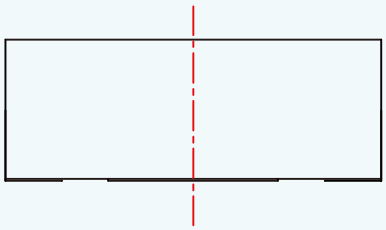


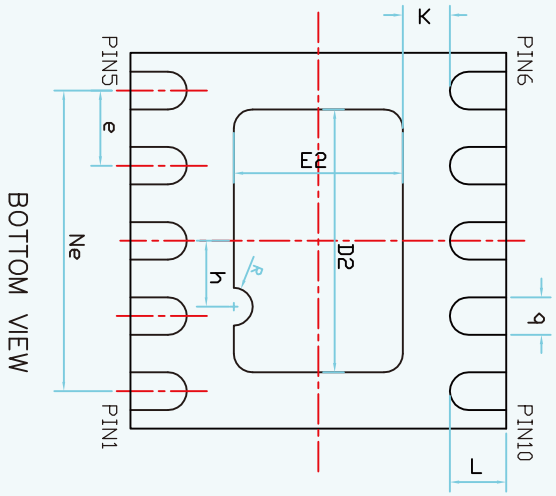
Package Information

IU7191T DFN2X2_10L(0202X0.75-0.40)



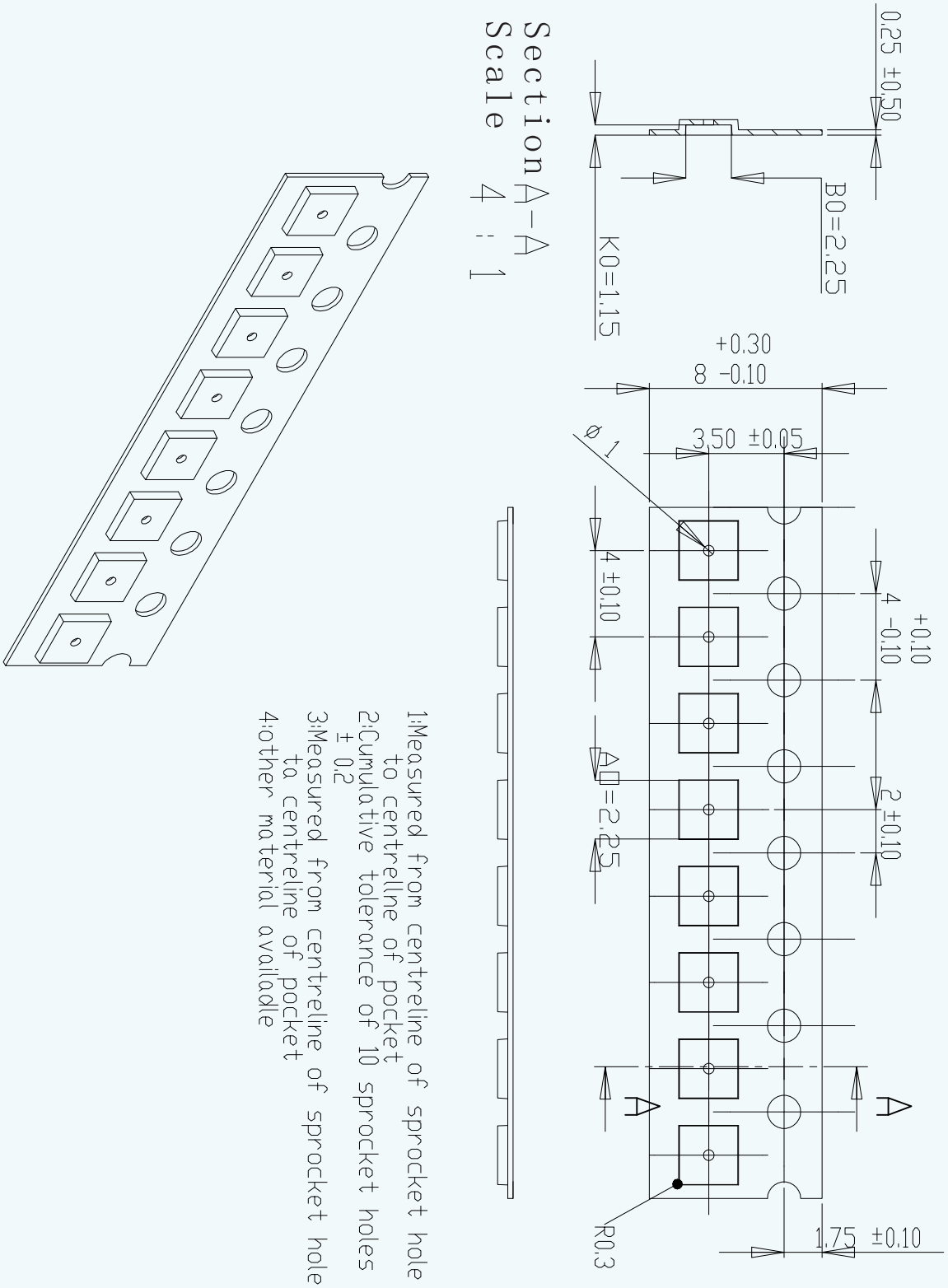






SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.203REF		
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
e	0.40BSC		
Ne	1.60BSC		
E	1.90	2.00	2.10
E2	0.80	0.90	1.00
L	0.25	0.30	0.35
h	0.30	0.35	0.40
R	0.05	0.10	0.15
K	0.20	0.25	0.30

TAPE AND REEL INFORMATION



1:Measured from centreline of sprocket hole to centrelline of pocket
2:Cumulative tolerance of 10 sprocket holes is ± 0.2
3:Measured from centreline of sprocket hole to centreline of pocket
4:other material available



Precautions for MOS Circuit Operation:

Static electricity can be generated in many places. The following precautions can effectively prevent MOS circuit from being damaged due to the sound of electrostatic discharge:

- Operators shall be grounded through anti-static wrist strap.
- The equipment enclosure must be grounded.
- Tools used during assembly must be grounded.
- Conductor packaging or anti-static materials must be used for packaging or transportation.

Declaration:
•Shanghai IXU Semiconductor Co., Ltd. reserves the right to make changes to the manual without prior notice! Customers should obtain the latest version of the material before use and verify whether the relevant information is complete and up-to-date.
•Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using products from Shanghai IXU Semiconductor Co., Ltd. for system design and complete machine manufacturing, in order to avoid potential risks of failure that may cause personal injury or property damage!
•The pursuit of enhancing product quality is endless. Shanghai IXU Semiconductor Co., Ltd. will wholeheartedly provide customers with even better products!