宽输入范围,低静态电流
兼容同步和异步外围应用,升压DC-DC控制器

概要

IU5708D是高性能宽输入范围（4.5V~40V）同步升压控制器，支持高达52V的输出电压。输出电压采用恒定频率电流模式脉宽调制（PWM）控制来实现调节。
芯片通过外部定时电阻器或通过与外部时钟信号同步来设置开关频率。在电阻编程模式下，开关频率可从50KHz编程到1MHz，也可以与300kHz至1MHz之间的外部时钟同步。
IU5708D包括一个6.6V栅极驱动电源，此电源适合于驱动很多类型的MOSFET，同步整流针对高电流应用而启用高效率，而且无损耗电感器DCR进一步提升了效率，是灵活的高功率密度且高可靠性的升压转换器解决方案。

描述

- 52V最大输出电压
- 4.5V~40V输入电压范围
- 针对标准阈值MOSFET优化的6.6V栅极驱动器
- 具有内部斜坡补偿的电流模式控制
- 与外部时钟的同步能力
- 50KHz至1MHz的可调频率
- 外部可调软启动时间
- 输出电压电源正常指示器
- ±1%反馈基准电压
- 6μA关断电源电流
- 720μA静态工作电流
- 逐周期电流限制和热关断
- 可调欠压闭锁(UVLO) 和输出过压保护

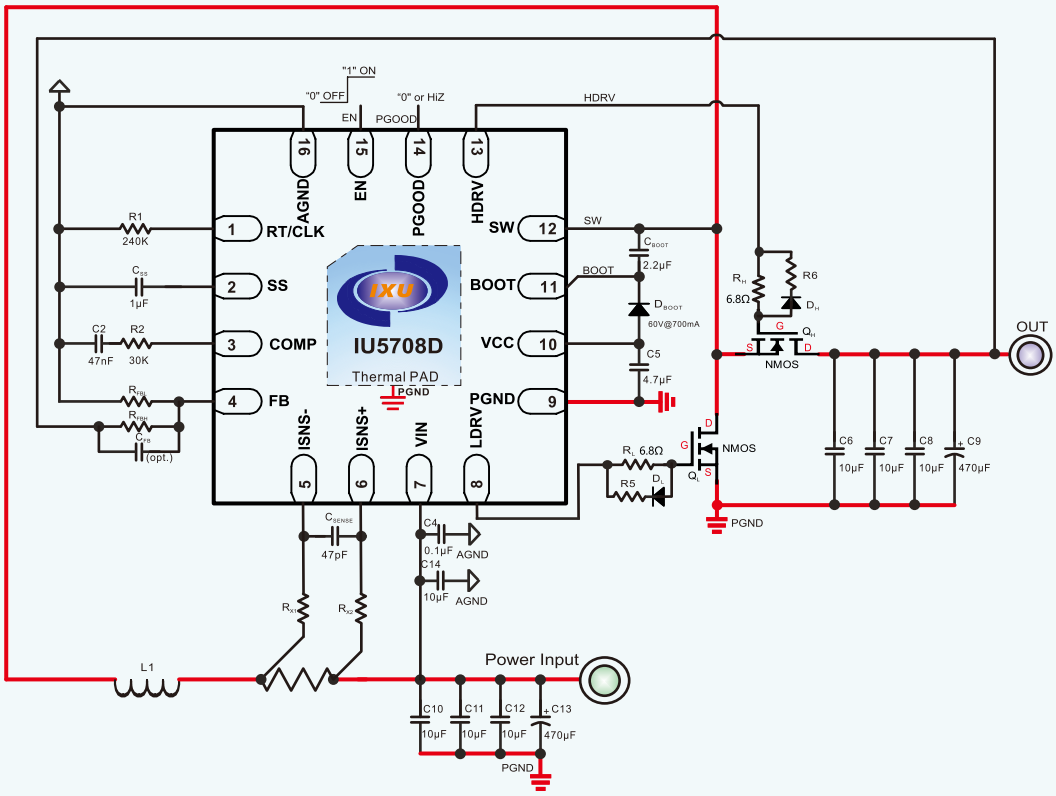
应用

- 用于PC的Thunderbolt 端口
- 汽车电源系统，电池供电系统
- 5V，12V 和24V DC 总线电源系统
- 氮化镓(GaN) 射频(RF) 功率放大器

封装

- QFN3X3_16L

典型应用图



IU5708D 同步应用电路图

备注:

（1）L1功率电感的饱和电流值须大于所设定的电感峰值电流，并留有足够余量。
（2）功率电阻R_{SENSE}用来设定电感峰值电流值，须紧靠其两端进行抽头。
（3）注意应用图中同步上管Q_H的源漏方向。
（4）D_{BOOT}选型为60V@700mA肖特基二极管。
（5）须从输入电源电容上单独引线到芯片第7脚。
（6）图中红色实线为流大电流路径。

Wide Input Range, Low IQ
Boost DC–DC Controller Compatible with Synchronous and Asynchronous Peripheral Applications

General Description

IU5708D is a high-performance wide input range (4.5V~40V) synchronous boost controller, supporting output voltages up to 52V. The output voltage is regulated by constant frequency current mode pulse width modulation (PWM) control.

The chip sets the switching frequency through an external timing resistor or by synchronizing with an external clock signal. In the resistor programming mode, the switching frequency can be programmed from 50KHz to 1MHz, and it can also be synchronized with an external clock between 300kHz and 1MHz.

IU5708D includes a 6.6V gate drive power supply, which is suitable for driving many types of MOSFETs. Synchronous rectification enables high efficiency for high-current applications, and the lossless inductor DCR further improves efficiency, making it a flexible high-power density and high-reliability boost converter solution.

Features

- 52V Maximum Output Voltage
- 4.5 to 40V VIN Range
- 6.6V Gate Drive Optimized for Standard Threshold MOSFET
- Current-Mode Control With Internal Slope Compensation
- Adjustable Frequency from 50 kHz to 1 MHZ
- Synchronization Capability to External Clock
- Adjustable Soft-Start Time
- Inductor DCR or Resistor Current Sensing
- Output Voltage Power-Good Indicator
- ±1% Feedback Reference Voltage
- 6μA Shutdown Supply Current
- 720μA Operating Quiescent Current
- Cycle-by-Cycle Current Limit and Thermal shutdown
- Adjustable Undervoltage Lockout (UVLO) and Output
- Overvoltage Protection

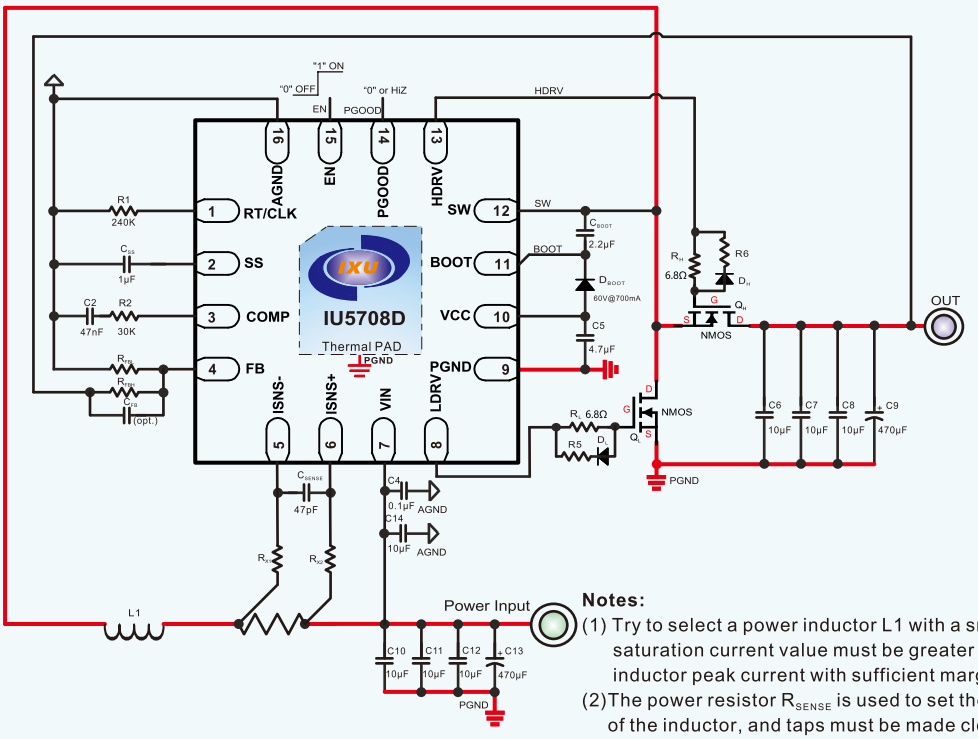
Applications

- Thunderbolt Port for PCs
- Automotive Power Systems, Synchronous Flyback
- GaN RF Power Amplifiers
- Tablet Computer Accessories
- Battery-Powered Systems
- 5-V, 12-V, and 24-V DC Bus Power Systems

Package

- QFN3X3_16L

Typical Application



IU5708D Synchronous Application Circuit Diagram

Notes:

(1) Try to select a power inductor L1 with a small DCR, and the saturation current value must be greater than the set inductor peak current with sufficient margin.

(2)The power resistor R_{SENSE} is used to set the peak current value of the inductor, and taps must be made close to its two ends.

(3) Pay attention to the source-drain direction of the synchronous high-side switch Q_H in the application diagram.

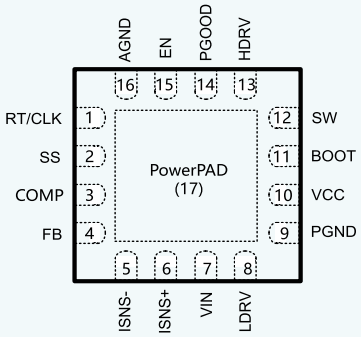
(4) The D_{BOOT} is selected as a 60V@700mA Schottky diode.

(5) A separate wire must be led from the input power supply capacitor to Pin 9 of the chip.

(6) The red solid line in the diagram indicates the large current path.

Pin Configuration and Functions

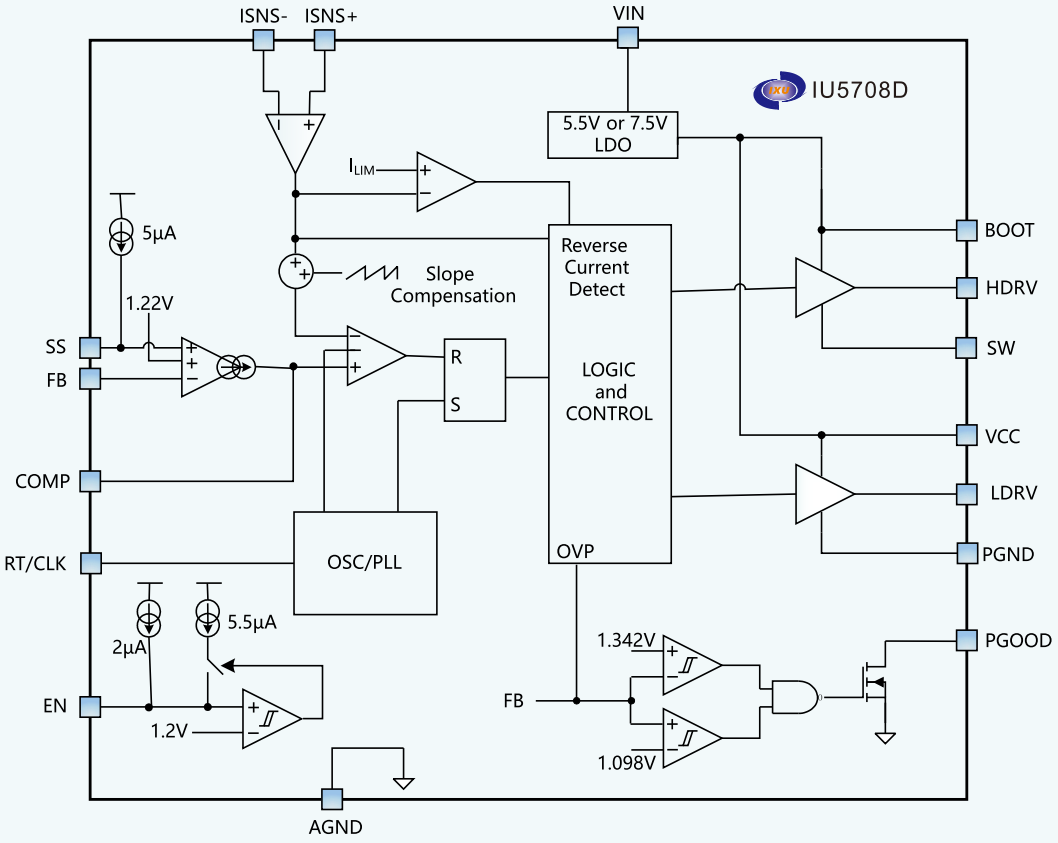
QFN3X3_16L(TOPVIEW)



BOTTOM VIEW

NAME	NO.	DESCRIPTION
RT/CLK	1	Resistor timing and external clock.An external resistor fromthis pin to the AGND pin programs the switching frequency between 50kHz and 1MHz.Driving the pin with an external clock between 300kHz to1MHz synchronizes the switching frequency to the external clock.
SS	2	Soft-start programming pin.Acapacitor between the SS pin and AGND pin sets soft-start time.
COMP	3	Output of the internal transconductance error amplifier.The feedback loop compensation network is connected from this pin to AGND.
FB	4	Error amplifier input and feedback pin for voltage regulation.Connect this pin to the center tap of a resistor divider to set the output voltage.
ISNS–	5	Inductor current sense comparator inverting input pin.
ISNS+	6	Inductor current sense comparatornon-inverting input pin.
VIN	7	The input supply pin to the IC.Connect VIN to a supply voltage between 4.5 and 40V.It is a cceptable for the voltage on the VIN pin to be different from the boost power stage input,ISNS+,and ISNS–pins.
LDRV	8	Low-side gate driver output.Connect this pin to the gate of the low-side N-channel MOSFET. When VIN bias is removed,an internal 200kΩ resistor pulls LDRV to PGND.
PGND	9	Power ground
VCC	10	Output of an internal LDO and power supply for internal control circuits and gate drivers.VCC is typically 7.5V Connect a low-ESR ceramic capacitor from this pin to PGND.IXU recommends a capacitance range from 0.47 to 10μF.
BOOT	11	Bootstrap capacitor node for high-side MOSFET gate driver.Connect the bootstrap capacitor from this pin to the SW pin.connect a bootstrap diode from VCC to BOOT.
SW	12	Switching node of the boost converter.Connect this pin to the junction of the drain of the low-side MOSFET, the source of high-side synchronous MOSFET,and the inductor.
HDRV	13	High-side gate driver output.Connect this pin to the gate of the high-side synchronous rectifier MOSFET.When VIN bias is removed,this pin is connected to SW through an internal 200kΩ resistor.
PGOOD	14	Power good indicator.This pin is an open-drain output.Recommends a10kΩ pullup resistor between PGOOD and VCC or an external logic supply pin.
EN	15	Enable pin with internal pullup current source.Floating this pin will enable the IC.Pull below 1.2V to enter low current standby mode.Pull below 0.4V to enter shutdown mode.The EN pin can be used to implement adjustable UVLO using two resistors.
AGND	16	Analog signal ground of the IC. AGND should be connected to PGND at a single point on the PCB.
PowerPAD	17	The PowerPAD should be connected to AGND. If possible, use thermal vias to connect to an internal ground plane for improved power dissipation.

Functional Block Diagram



Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
Voltage	VIN,EN,ISNS+,ISNS–,HDRV,LDRV,BOOT	–0.3	43	V
	DC voltage:SW	–0.6	55	V
	Transient voltage (10ns max):SW	–2	55	V
	FB,RT/CLK,COMP,SS,FB	–0.3	6.0	V
	BOOT,HDRV voltage with respect to ground		55	V
	BOOT,HDRV voltage with respect to SW pin		8	V
	PGOOD	–0.3	24	V
Operating junction temperature		–40	150	°C

Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	4.5		40	V
V_{OUT}	Output voltage range	V_{IN}		52	V
V_{EN}	EN voltage range	0		42	V
V_{CLK}	External switching frequency logic input range	0		3.6	V
T_J	Operating junction temperature	–40		150	°C

Thermal Characteristics[2]

THERMALMETRIC		QFN3X3_16L	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	49	

Ordering and Marking Information

Device	Package Type	Device Marking	Reel Size	Tape Width	Quantity
IU5708D	QFN3X3_16L		13''	12mm	3000 units

ESD Susceptibility

ESD Susceptibility-HBM ---------- ±2kV

ESD Susceptibility-MM ---------- ±200V

1. The above parameters are only the limit values of device operation. It is not recommended that the working conditions of the device exceed the limit values. Otherwise, the reliability and life of the device will be affected, and even permanent damage will be caused.
2. Where the PCB board is placed in IU5708D, a heat dissipation design is needed. The heat sink at the bottom of IU5708D is connected with the heat sink area of PCB board.

Electrical Characteristics (V_{IN}=4.5V~38V ， T_A=25℃, unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply and Enable						
V_{IN}	Input power voltage		4. 5		40	V
VIN_{UV}	VIN undervoltage protection threshold	VIN Falling		3.9		V
ΔVIN_{UV}	VIN undervoltage protection hysteresis			200		mV
I_Q	Chip static working current	non-switching R_T= 115KΩ, V_{FB}= 2V		720		μA
I_{SD}	Chip off current	V_{EN}=0.4V		2.5	6	μA
V_{EN}	EN standby threshold	V_{EN} Falling	0.4	0.7	0.9	V
	EN on threshold	V_{EN} Rising		1.2		V
	EN off threshold	V_{EN} Falling		1.125		V
I_{EN}	EN Pull-up current	V_{EN} =1V		2		μA
	EN hysteresis current	V_{EN} =1.3V		5.5		μA
t_{EN}	EN turn on time			125		μs
V_{CC}	VCC voltage	VIN=12~24V, I_{VCC} =0		6.6		V
		VIN=4.5V, I_{VCC} =0		4.5		V
I_{VCC}	VCC maximum output current		50			mA
Reference Voltage and Error Amplifier						
V_{REF}	Feedback voltage reference		1.188	1.2	1.212	V
I_{FB}	Error amplifier input bias current			20		nA
I_{COMP}	Sink current at COMP port	V_{FB}=V_{REF}+ 250mV, V_{COMP} =1.5V		24		uA
	Source current at COMP port	V_{FB}=V_{REF}- 250mV, V_{COMP} =1.5V		160		uA
V_{CLAMP}	COMP port clamping voltage	High clamp V_{FB} =1V		2.04		V
		Low clamp V_{FB} =1.5V		0.68		V
	COMP port threshold	Duty cycle = 0%		1		V

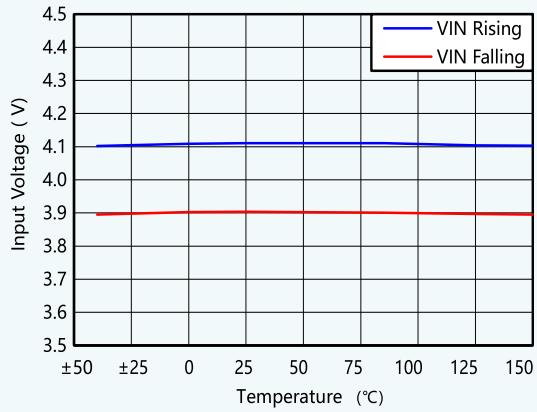
Electrical Characteristics (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{ea}	Error amplifier transconductance			210		uS
R_{ea}	Error amplifier output impedance			95		MΩ
F_{ea}	Error amplifier crossover frequency			2		MHz
Current Detection						
V_{CSmax}	**Maximum current detection threshold**	At 0% Duty Cycle		73		mV
		At Max Duty Cycle		61		mV
V_{RCsns}	Reverse current detection threshold			3		mV
I_{SNS+}	Sense+ port current			95		uA
I_{SNS-}	Sense- port current			70		uA
RT/CLK						
f_{SW}	Switching frequency	Resistor timing mode	50		1000	KHz
		R_T=100KΩ		595		KHz
		R_T =75KΩ		750		KHz
$V_{RT/CLK}$	**RT/CLK port voltage**			0.5		V
f_{CLK}	**Phase-locked loop frequency synchronization range**		300		1000	KHz
Power Switch Drive						
R_{LDRV}	LDRV Pull-up impedance	V_{IN} = 12 V ~ 24 V		2		Ω
		V_{IN} = 4.5 V		2.4		Ω
	LDRV Pull-down impedance	V_{IN} = 12 V ~ 24 V		1.22		Ω
		V_{IN} = 4.5 V		1.37		Ω
R_{HDRV}	HDRV Pull-up impedance	V_{IN} = 12 V ~ 24 V		2		Ω
		V_{IN} = 4.5 V		2.2		Ω
	HDRV Pull-down impedance	V_{IN} = 12 V ~ 24 V		1.25		Ω
		V_{IN} = 4.5 V		1.76		Ω

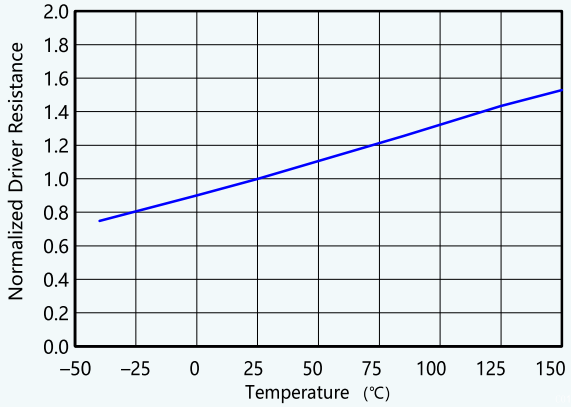
Electrical Characteristics (continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD, SS , OVP						
P_{GDL}	POOD low level threshold	V_{FB} falling		90%		
	POOD low level hysteresis			2%		
P_{GDH}	POOD high level threshold	V_{FB} rising		110%		
	POOD high level hysteresis			2%		
P_{GDSC}	PGOOD sink current	V_{PGOOD} = 0.4 V	1.8	4		mA
P_{GDLK}	PGOOD pin leakage current	V_{PGOOD} = 7 V		100		nA
V_{IN_PGD}	Minimum V_{IN} for valid PGOOD			2.5	4.3	V
I_{SS}	Soft start bias current	V_{SS}= 0 V		5		uA
R_{SS}	**Soft start discharge resistance**			250		Ω
V_{OVP}	**Overvoltage protection threshold**	V_{FB} rising		107%		
	Overvoltage protection hysteresis			2%		
Temperature Protection						
T_{SD}	Over temperature protection threshold			160		℃
T_{hyst}	Overtemperature protection hysteresis			20		℃

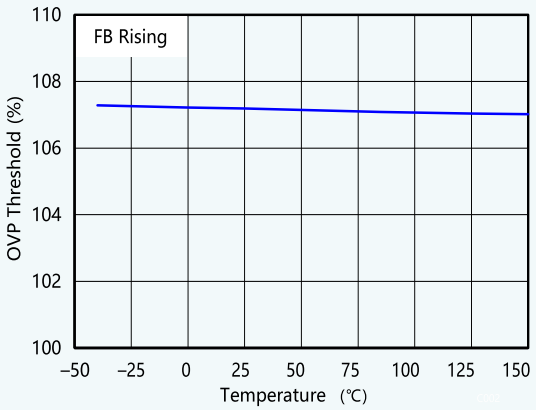
Typical Operating Characteristics (V_{IN}= 12V, f_{SW}= 500 KHz ,T_A = 25°C unless otherwise noted)



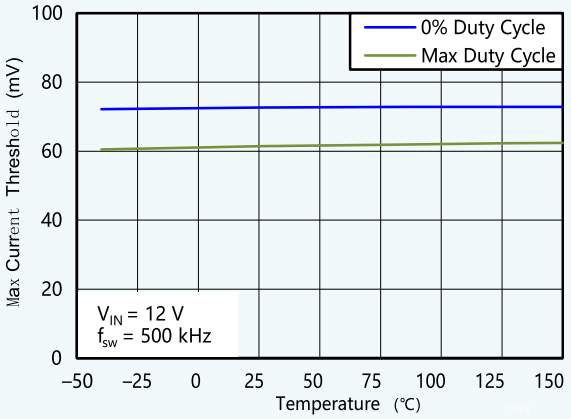
Input Start and Stop Voltage vs Temperature



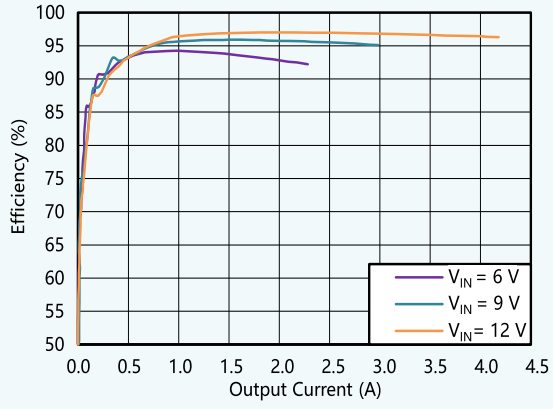
Gate Driver Output Resistance vs Temperature



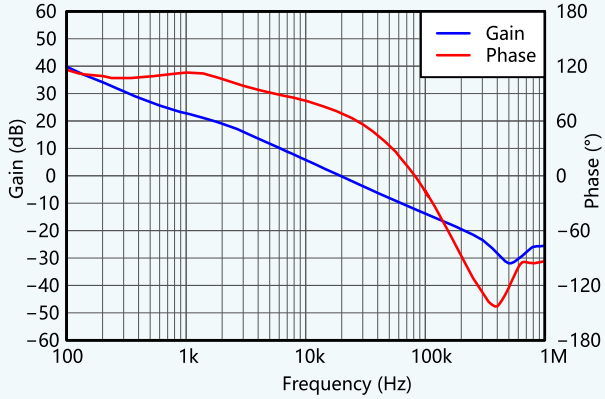
OVP Threshold vs Temperature



Maximum Current Sense Threshold vsTemperature



Efficiency vs Output Current



Loop Gain and Phase

IU5708D Application Points

1. Operation process

The PWM control circuit in IU5708D turns on the low-side MOSFET at the beginning of each oscillator clock cycle, and the error amplifier compares the output voltage feedback signal at the FB pin with the internal reference voltage. When the inductance current reaches the threshold level set by the error amplifier output, the low-side MOSFET turns off. The high-side MOSFET is turned on until the beginning of the next oscillator clock cycle or until the inductive current reaches the reverse current detection threshold. When the low-side MOSFET is in partial switching period, the input voltage is applied to both ends of the inductor, and the energy is stored as the inductor current rises. At the same time, the output capacitor provides the load current. When the low-side MOSFET is turned off by the PWM controller, the inductor transmits the stored energy through the external synchronous tube to supplement the output capacitor and provide the load current. This operation is repeated at each switch cycle. The chip has internal slope compensation function to avoid mode control when the inherent subharmonic oscillation duty cycle of peak current is higher than 50%. At the same time, it also has the functions of externally adjustable soft start time, output voltage power supply normal (POWER GOOD) indication, cycle by cycle current limit and overheat protection.

2. Switching Frequency

The switching frequency is set by the resistor (RT) connected to the RT/CLK pin of the chip, and can also be synchronized with the external clock applied to the RT/CLK pin. This external clock should be in the range of 300KHz to 1MHz. The logic level required by the external clock is shown in the electrical parameter table. The pulse width of the external clock should be greater than 20ns to ensure correct synchronization. When the chip is synchronized with the external clock, a 60KΩ~1150KΩ resistor must be connected between the RT/CLK pin and the ground. This pin cannot be floated empty.

$$f_{SW}(KHz) = \frac{59500}{R_T(K\Omega)}$$

3. LDO

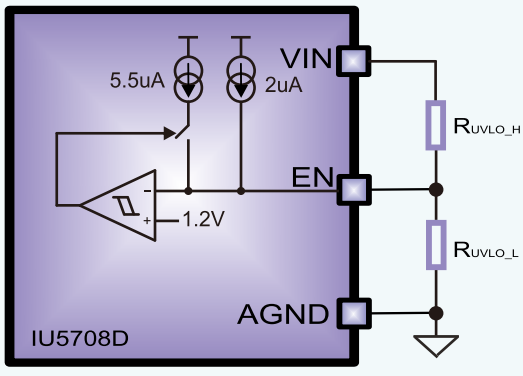
The Iu5708D contains a low voltage differential regulator, which provides bias power for the controller and grid driver. The LDO output of the chip is adjusted to 6.6V. When the input voltage is lower than the VCC regulation level, the VCC output tracks the VIN voltage. The output current of VCC regulator should not exceed 50mA. The capacitance of VCC pin depends on the whole system design and its startup characteristics. The recommended range capacitance value is 0.47μF to 10μF。

4. Undervoltage Detection (UV)

The chip undervoltage detection circuit can prevent the equipment from misoperation under the input voltage lower than 3.9V (typical). When the input voltage is below the VINUV threshold, the internal PWM control circuit and the grid driver are closed. This threshold is set to 4.5V below the minimum operating voltage to ensure that the instantaneous VIN drop will not cause the chip to reset. For input voltage between UV threshold and 4.5V, the chip tries to work, but cannot ensure electrical specifications. The EN pin can be used to realize adjustable UVLO, if the expected starting threshold is higher than 3.9V. Details will be provided in the following sections.

5. Enable and Set Under Voltage Lockout (UVLO)

The EN pin voltage must be greater than 1.2V (typical) to turn on the chip. When the EN voltage is less than 0.4V, the chip enters the shutdown mode. In the shutdown mode, the input power current of the chip is less than 6μA。 EN pin has internal 2μA pull-up current source. When the EN pin is floating, the current source provides default enabling conditions. When the EN pin voltage is higher than the shutdown threshold but lower than 1.2V, the chip is in standby mode. The EN pin can be used to realize the adjustable input UVLO. As shown in the figure, use the voltage divider from VIN pin to AGND to set the UVLO level. Once the EN pin voltage exceeds 1.2V (typical) threshold voltage, the EN pin will generate an additional 5.5μA Hysteresis current. When the EN pin voltage is lower than 1.14V (typical value), the hysteresis current will be eliminated. Adding hysteresis current at the EN threshold helps to adjust the input voltage hysteresis. RUVLO_ H and RUVLO_ L is calculated as follows.



$$R_{UVLO\_H} = \frac{V_{START} * \frac{V_{EN\_DIS}}{V_{EN\_ON}} - V_{STOP}}{I_{EN\_pup} * (1 - \frac{V_{EN\_DIS}}{V_{EN\_ON}}) + I_{EN\_hys}}$$

$$R_{UVLO\_L} = \frac{R_{UVLO\_H} * V_{EN\_DIS}}{V_{STOP} - V_{EN\_DIS} + R_{UVLO\_H} * (I_{EN\_pup} + I_{EN\_hys})}$$

In the above formula:

- V_{START} is the preset VIN pin on voltage;
- V_{STOP} is the preset VIN pin off voltage;
- V_{EN_ON} is the EN pin enabling on voltage, 1.2V (TYP);
- V_{EN_DIS} is the EN pin enabling off voltage, 1.14V(TYP);
- I_{EN_hys} is the built-in hysteresis current of EN pin , 5.5uA(TYP);
- I_{EN_pup} is the built-in pull-up current of EN pin , 2uA(TYP);

6. Set Output Voltage

The internal reference voltage provides an accurate 1.2V voltage at the same phase end of the error amplifier. To set the output voltage, select FB pin voltage divider R_{FBH} and R_{FBL} according to the following formula.

$$V_{OUT}(V) = (\frac{R_{FBH}}{R_{FBL}} + 1) * 1.2$$

7. Soft Start

The chip has a built-in soft start circuit, which can significantly reduce the start current spike and output voltage overshoot. When the IC is enabled, the internal bias current source (typical value is 5μA) Charge the capacitor CSS on the SS pin. When the SS pin voltage is less than the internal 1.2V reference voltage, the FB pin voltage will be adjusted to the SS pin voltage instead of the internal 1.2V reference voltage. Once the SS pin voltage exceeds the reference voltage, the equipment will adjust the FB pin voltage to 1.2V. The soft start time of output voltage can be calculated by the following formula.

$$t_{SS}(mS) = \frac{1.2(V)}{5(uA)} * C_{SS}(nF)$$

8. POWER GOOD Indication

The PGOOD pin of the chip indicates whether the output voltage is within the preset range by monitoring the FB pin voltage. If this function is not used, the pin can be directly grounded or floating.

- When the output voltage is within ±10% of the set value, the PGOOD pin output is 0.
- When the output voltage is not within ±10% of the set value, the PGOOD pin output is in high resistance state. PGOOD pin can be pulled up to 24V voltage source by external resistance (10KΩ ~100KΩ recommended).

9. Output Overvoltage Protection

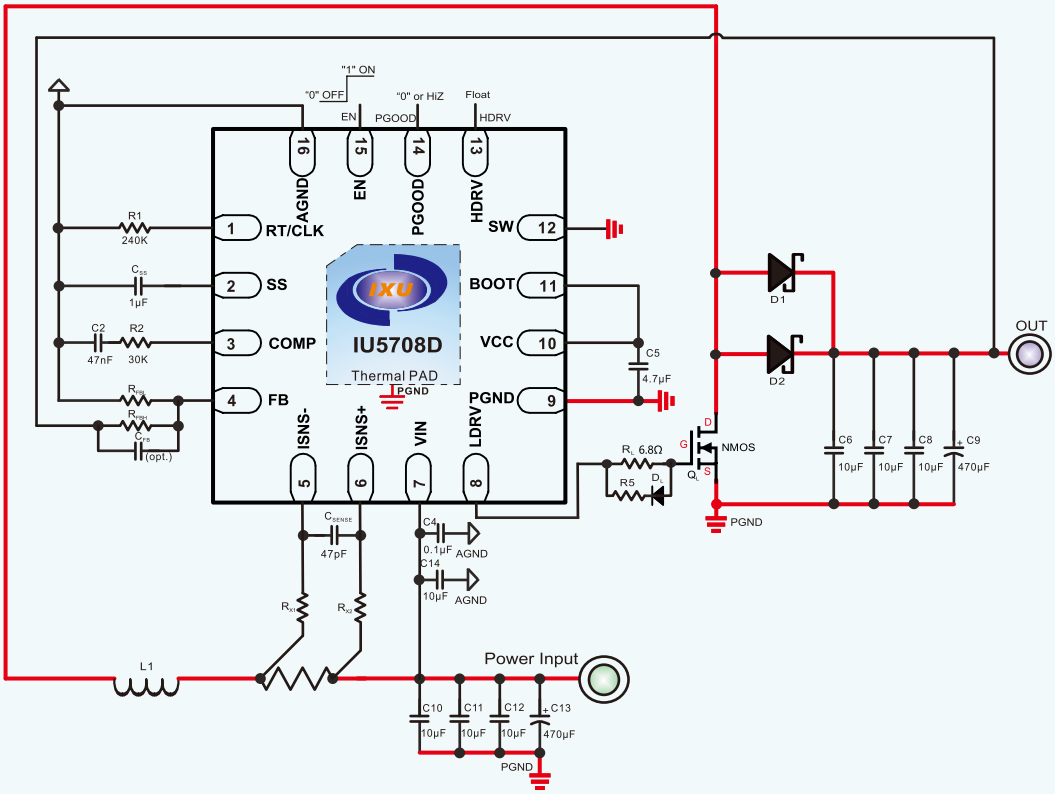
The chip integrates an overvoltage protection (OVP) circuit. When the output voltage reaches the OVP threshold (107% of the output voltage set value is fixed internally), the circuit turns off the low-side MOSFET. When the output voltage drops below 105% of the output voltage setting value, the low side MOSFET returns to normal PWM control. The OVP circuit protects the power MOSFET and minimizes the output voltage overshoot under transient or fault conditions.

10. Selection of Overcurrent Protection

The chip provides current limit protection cycle by cycle. When the inductive current reaches the current limit threshold, the low-side MOSFET is turned off. The current limiting circuit is reset at the beginning of the next switching cycle. During the overcurrent period, the output voltage begins to decrease with the output load. The chip has built-in slope compensation circuit to prevent sub-harmonic oscillation under high duty cycle. The slope compensation will reduce the overcurrent limit threshold (maximum current detection threshold) as the duty cycle increases.Maximum inductive current detection threshold V_{CSmax} sets the maximum peak inductive current, which is the maximum average inductive (input) current I_{ave_max} and half inductive ripple peak (ΔI_L). The detection resistance value shall be selected according to the required maximum input current and ripple current and calculated using the following formula.

$$R_{SENSE} = \frac{V_{CSmax}}{I_{ave\_max} + \frac{\Delta I_L}{2}}$$

IU5708D Asynchronous Application



IU5708D Asynchronous Application Circuit Diagram

Notes:

(1) Try to select a power inductor L1 with a small DCR, and the saturation current value must be greater than the set inductor peak current with sufficient margin.

(2)The power resistor R_{SENSE} is used to set the peak current value of the inductor, and taps must be made close to its two ends.

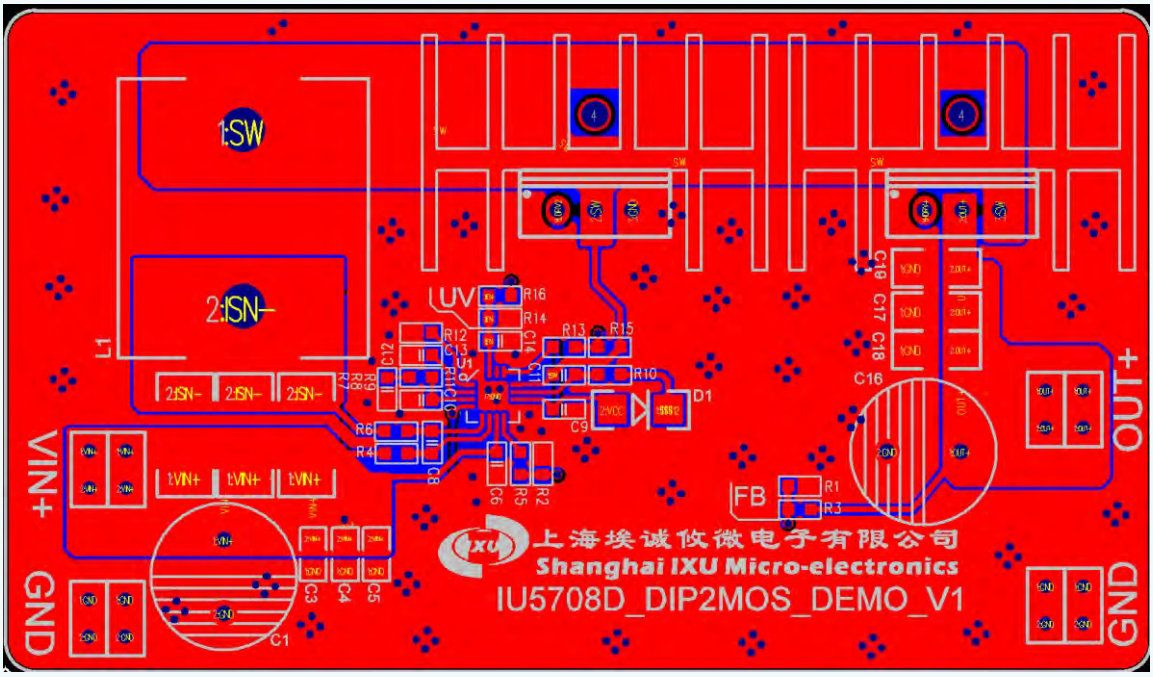
(3) The saturation current value of Schottky diodes D1 and D2 after parallel connection must be greater than the set inductor peak current with sufficient margin.

(4) A separate wire must be led from the input power supply capacitor to Pin 7 of the chip.

(5) The red solid line in the diagram indicates the large current path.

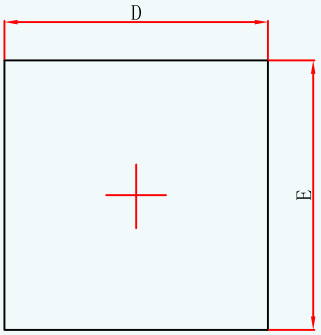
PCB Layout Recommendations

Please refer to our company's Demo layout and routing as much as possible.

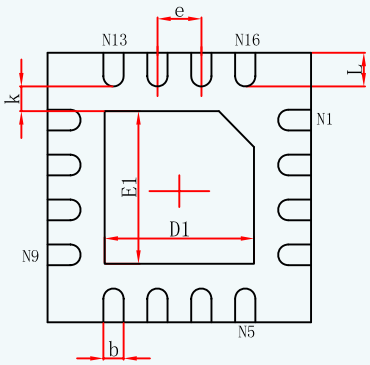


Package information

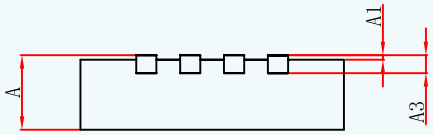
IU5708D QFN 3X3_16L



Top View



Bottom View



Side View

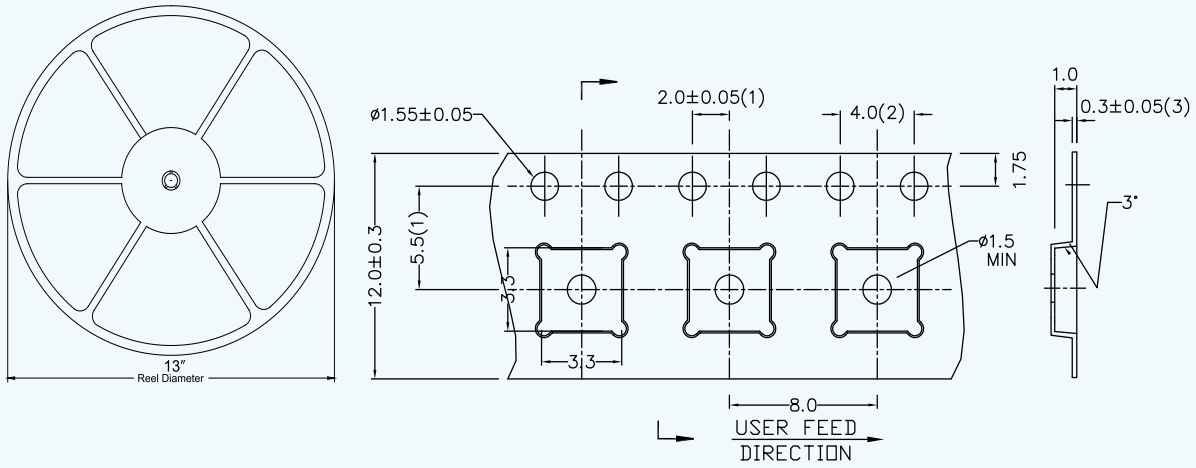
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	1.600	1.800	0.063	0.071
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.500	0.012	0.020

Notes:

(1) All dimensions are in millimeters.
(2) Complies with JEDEC standard MO-220.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



Precautions for MOS Circuit Operation:

Static electricity can be generated in many places. The following precautions can effectively prevent MOS circuit from being damaged due to the sound of electrostatic discharge:

- Operators shall be grounded through anti-static wrist strap.
- The equipment enclosure must be grounded.
- Tools used during assembly must be grounded.
- Conductor packaging or anti-static materials must be used for packaging or transportation.

Declaration:

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