Wide Input Range, Low IQ

Boost DC–DC Controller Compatible with Synchronous and Asynchronous Peripheral Applications

General Description

IU5706E is a high performance wide input range (4.5V~24V) synchronous boost controller that supports up to 33V output voltage. The output voltage is controlled by a constant frequency current mode pulse width modulation (PWM).The chip sets the switch frequency either by an external timer resistor or by synchronizing with the external clock signal. In resistor programming mode, the switch frequency can be programmed from 50KHz to 1MHz, or synchronized with an external clock between 300KHz and 1MHz. Synchronous rectifier enables high efficiency for high current applications, and lossless inductor DCR further enhances efficiency. IU5706E includes a 6.6V grid-driven power supply suitable for driving many types of MOSFETs.

Package

- EQA16

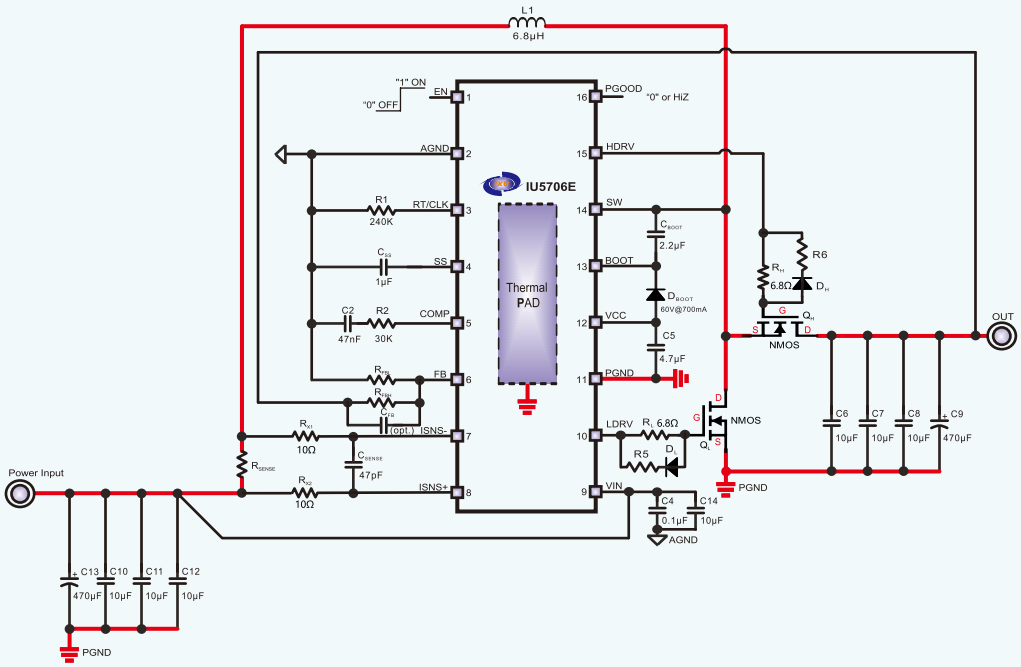
Features

- 33V Maximum Output Voltage
- 4.5V to 24V Input Voltage Range
- Current Mode with Internal Slope Compensation
- Synchronization with External Clock
- Adjustable Frequency from 50KHz to 1MHz
- External Adjustable Soft Start Time
- Output Voltage Power Supply Normal Indicator
- ±1% Feedback Reference Voltage
- 6μA Power off Current
- 720μA Static Working Current
- Periodic Current Limit and Thermal Shutdown
- Adjustable Undervoltage Lockout (UVLO) and Output Overvoltage Protection

Applications

- Thunderbolt Port for PC
- Automotive Power System
- Battery Power System
- 5V, 12V and 24V DC Bus Power System

Typical Application



IU5706E Synchronous Application Circuit Diagram

Notes:

(1) Try to select a power inductor L1 with a small DCR, and the saturation current value must be greater than the set inductor peak current with sufficient margin.

(2)The power resistor R_{SENSE} is used to set the peak current value of the inductor, and taps must be made close to its two ends.

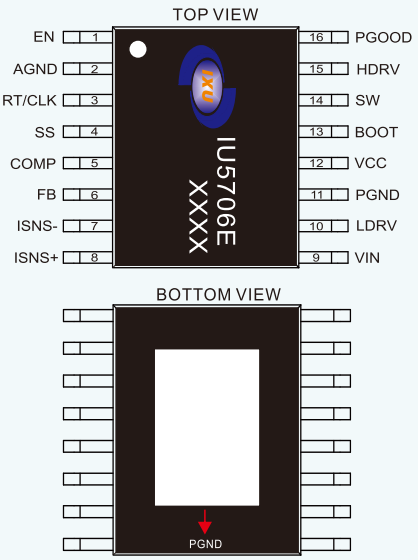
(3) Pay attention to the source-drain direction of the synchronous high-side switch Q_H in the application diagram.

(4) The D_{BOOT} is selected as a 60V@700mA Schottky diode.

(5) A separate wire must be led from the input power supply capacitor to Pin 9 of the chip.

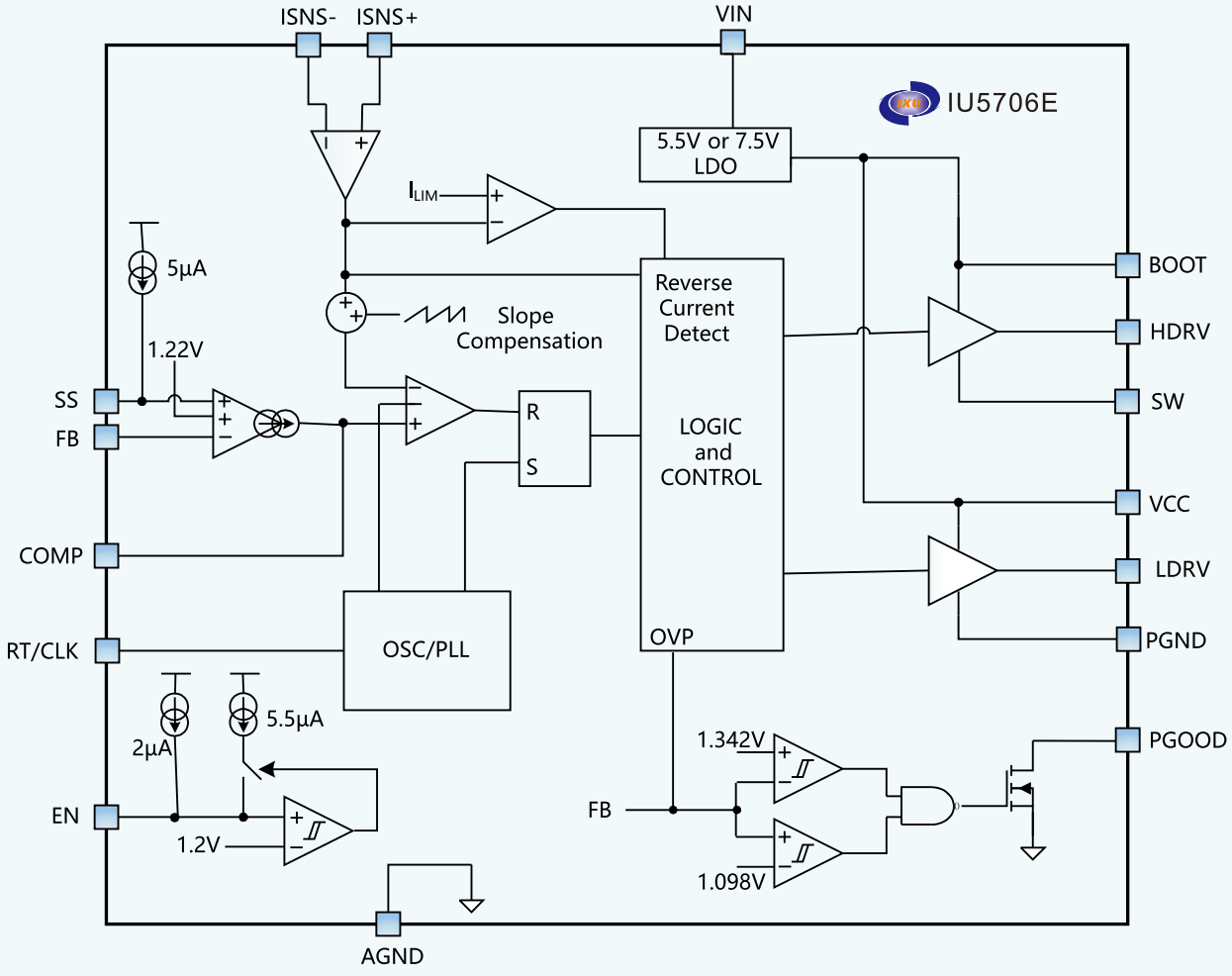
(6) The red solid line in the diagram indicates the large current path.

PIN Configuration and Functions



PIN	NAME	DESCRIPTION
1	EN	Enable pin with internal pull-up current source, floating this pin will enable IC
2	AGND	Analog ground
3	RT/CLK	Resistor timing and external clock interface
4	SS	Soft start programming pin, capacitor between SS pin and AGND pin set soft start time
5	COMP	The output of the internal transconductance error amplifier, from which the feedback loop compensation network is connected to the AGND
6	FB	Error amplifier input and feedback pins for voltage regulation. Connect this pin to the center tap of the resistance voltage divider to set the output voltage
7	ISNS-	The negative input pin of the inductive current detection comparator is usually connected to the negative input pin of the inductive current detection comparator
8	ISNS+	The positive input pin of the inductive current detection comparator, which is usually connected to the VIN side of the current detection resistor
9	VIN	Input power supply
10	LDRV	Low-side gate driver output
11	PGND	Power-ground
12	VCC	Output of internal LDO and power supply of internal control circuit and gate driver
13	BOOT	High-side gate driver bootstrap capacitor node of grid driver
14	SW	Switch node of boost converter
15	HDRV	High-side gate driver output
16	PGOOD	Output voltage power indicator, this pin is open drain output

Functional Block Diagram



Absolute Maximum Ratings[1]

SYMBOL	PARAMETER	VALUE	UNIT
VMAX	EN, ISNS-, ISNS+, VIN, LDRV, HDRV, SW, BOOT	-0.3~40	V
	PGOOD	-0.3~24	V
	VCC	-0.3~12	V
	RT/CLK, SS, COMP, FB	-0.3~6	V
T_J	Junction operating temperature range	-40~150	℃
T_{STG}	Storage temperature range	-60~150	℃
T_{SDR}	Lead temperature (Soldering, 10 sec.)	260	℃

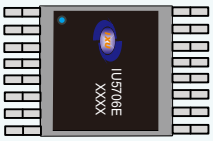
Recommended Operating Conditions

SYMBOL	PARAMETER	VALUE	UNIT
V_{IN}	Input voltage range	4.5 ~ 24	V
V_{OUT}	Output voltage range	V_{IN} ~ 33	V
V_{EN}	Enable voltage range	0 ~ V_{IN}	V
V_{CLK}	External switch frequency logic input range	0 ~ 3.6	V
T_J	Junction operating temperature range	-40~125	℃
T_A	Ambient temperature range	-40~85	℃

Ordering Information

SYMBOL	PARAMETER	VALUE	UNIT
θ_{JA}(EQA16)	Package thermal resistance - chip to environment thermal resistance	45	℃/W
θ_{JC}(EQA16)	Package thermal resistance - chip to package surface thermal resistance	10	℃/W

Ordering Information

Product Name	Package Type	Device Marking	Reel Size (Inch)	Tape width	Quantity
IU5706E	EQA16		13″	12mm	4000 per Reel
			Tube		100

ESD Range

HBM (Human Body Model) ---------- ±2kV

MM (Machine model) ---------- ±200V

1. The above parameters are only the limit values of device operation. It is not recommended that the working conditions of the device exceed the limit values. Otherwise, the reliability and life of the device will be affected, and even permanent damage will be caused.
2. Where the PCB board is placed in IU5706E, a heat dissipation design is needed. The heat sink at the bottom of IU5706E is connected with the heat sink area of PCB board.

Electrical Characteristics (V_{IN}=4.5V~24V， T_A=25℃, unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply and Enable						
V_{IN}	Input power voltage		4. 5		24	V
VIN_{UV}	VIN undervoltage protection threshold	VIN Falling		3.9		V
ΔVIN_{UV}	VIN undervoltage protection hysteresis			200		mV
I_Q	Chip static working current	non-switching R_T= 115KΩ, V_{FB}= 2V		720		μA
I_{SD}	Chip off current	V_{EN}=0.4V		2.5	6	μA
V_{EN}	EN standby threshold	V_{EN} Falling	0.4	0.7	0.9	V
	EN on threshold	V_{EN} Rising		1.2		V
	EN off threshold	V_{EN} Falling		1.125		V
I_{EN}	EN Pull-up current	V_{EN} =1V		2		μA
	EN hysteresis current	V_{EN} =1.3V		5.5		μA
t_{EN}	EN turn on time			125		μs
V_{CC}	VCC voltage	VIN=12~24V, I_{VCC} =0		6.6		V
		VIN=4.5V, I_{VCC} =0		4.5		V
I_{VCC}	VCC maximum output current		50			mA
Reference Voltage and Error Amplifier						
V_{REF}	Feedback voltage reference		1.188	1.2	1.212	V
I_{FB}	Error amplifier input bias current			20		nA
I_{COMP}	Sink current at COMP port	V_{FB}=V_{REF}+ 250mV, V_{COMP} =1.5V		24		uA
	Source current at COMP port	V_{FB}=V_{REF}- 250mV, V_{COMP} =1.5V		160		uA
V_{CLAMP}	COMP port clamping voltage	High clamp V_{FB} =1V		2.04		V
		Low clamp V_{FB} =1.5V		0.68		V
	COMP port threshold	Duty cycle = 0%		1		V

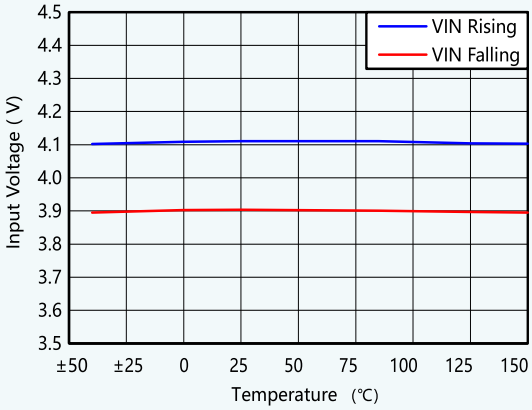
Electrical Characteristics (V_{IN}=4.5V~24V， T_A=25℃, unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{ea}	Error amplifier transconductance			210		uS
R_{ea}	Error amplifier output impedance			95		MΩ
F_{ea}	Error amplifier crossover frequency			2		MHz
Current Detection						
V_{CSmax}	**Maximum current detection threshold**	At 0% Duty Cycle		73		mV
		At Max Duty Cycle		61		mV
V_{RCsns}	Reverse current detection threshold			3		mV
I_{SNS+}	Sense+ port current			95		uA
I_{SNS-}	Sense- port current			70		uA
RT/CLK						
f_{SW}	Switching frequency	Resistor timing mode	50		1000	KHz
		R_T=100KΩ		595		KHz
		R_T =75KΩ		750		KHz
$V_{RT/CLK}$	**RT/CLK port voltage**			0.5		V
f_{CLK}	**Phase-locked loop frequency synchronization range**		300		1000	KHz
Power Switch Drive						
R_{LDRV}	LDRV Pull-up impedance	V_{IN} = 12 V ~ 24 V		2		Ω
		V_{IN} = 4.5 V		2.4		Ω
	LDRV Pull-down impedance	V_{IN} = 12 V ~ 24 V		1.22		Ω
		V_{IN} = 4.5 V		1.37		Ω
R_{HDRV}	HDRV Pull-up impedance	V_{IN} = 12 V ~ 24 V		2		Ω
		V_{IN} = 4.5 V		2.2		Ω
	HDRV Pull-down impedance	V_{IN} = 12 V ~ 24 V		1.25		Ω
		V_{IN} = 4.5 V		1.76		Ω

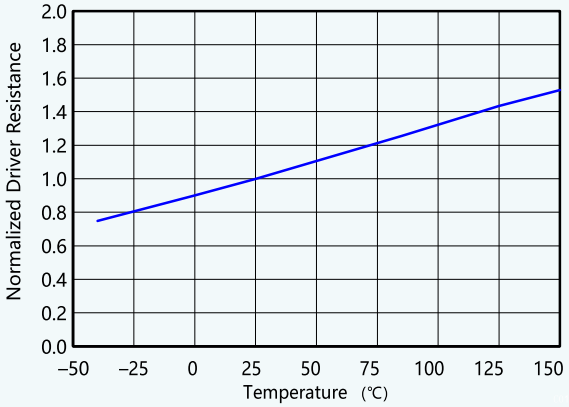
Electrical Characteristics (V_{IN}=4.5V~24V， T_A=25℃, unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD, SS , OVP						
P_{GDL}	POOD low level threshold	V_{FB} falling		90%		
	POOD low level hysteresis			2%		
P_{GDH}	POOD high level threshold	V_{FB} rising		110%		
	POOD high level hysteresis			2%		
P_{GDSC}	PGOOD sink current	V_{PGOOD} = 0.4 V	1.8	4		mA
P_{GDLK}	PGOOD pin leakage current	V_{PGOOD} = 7 V		100		nA
V_{IN_PGD}	Minimum V_{IN} for valid PGOOD			2.5	4.3	V
I_{SS}	Soft start bias current	V_{SS}= 0 V		5		uA
R_{SS}	**Soft start discharge resistance**			250		Ω
V_{OVP}	**Overvoltage protection threshold**	V_{FB} rising		107%		
	Overvoltage protection hysteresis			2%		
Temperature Protection						
T_{SD}	Over temperature protection threshold			160		℃
T_{hyst}	Overtemperature protection hysteresis			20		℃

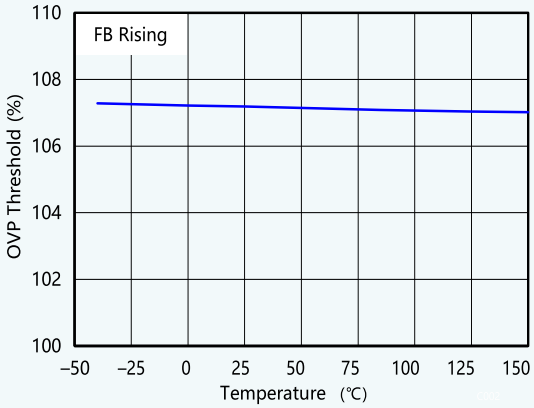
Typical Operating Characteristics (V_{IN}= 12V, f_{SW}= 500 KHz ,T_A = 25°C unless otherwise noted)



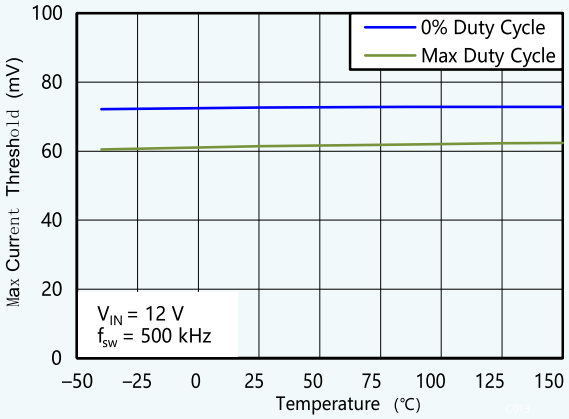
Input Start and Stop Voltage vs Temperature



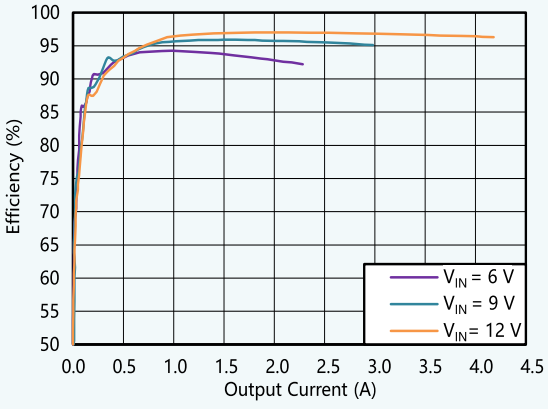
Gate Driver Output Resistance vs Temperature



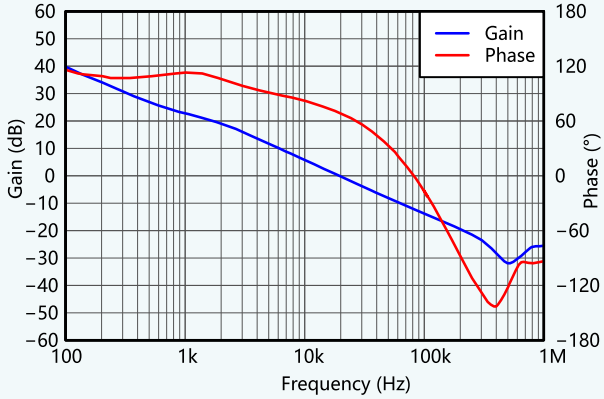
OVP Threshold vs Temperature



Maximum Current Sense Threshold vsTemperature



Efficiency vs Output Current



Loop Gain and Phase

IU5706E Application Points

1. Operation process

The PWM control circuit in IU5706E turns on the low-side MOSFET at the beginning of each oscillator clock cycle, and the error amplifier compares the output voltage feedback signal at the FB pin with the internal reference voltage. When the inductance current reaches the threshold level set by the error amplifier output, the low-side MOSFET turns off. The high-side MOSFET is turned on until the beginning of the next oscillator clock cycle or until the inductive current reaches the reverse current detection threshold. When the low-side MOSFET is in partial switching period, the input voltage is applied to both ends of the inductor, and the energy is stored as the inductor current rises. At the same time, the output capacitor provides the load current. When the low-side MOSFET is turned off by the PWM controller, the inductor transmits the stored energy through the external synchronous tube to supplement the output capacitor and provide the load current. This operation is repeated at each switch cycle. The chip has internal slope compensation function to avoid mode control when the inherent subharmonic oscillation duty cycle of peak current is higher than 50%. At the same time, it also has the functions of externally adjustable soft start time, output voltage power supply normal (POWER GOOD) indication, cycle by cycle current limit and overheat protection.

2. Switching Frequency

The switching frequency is set by the resistor (RT) connected to the RT/CLK pin of the chip, and can also be synchronized with the external clock applied to the RT/CLK pin. This external clock should be in the range of 300KHz to 1MHz. The logic level required by the external clock is shown in the electrical parameter table. The pulse width of the external clock should be greater than 20ns to ensure correct synchronization. When the chip is synchronized with the external clock, a 60KΩ~1150KΩ resistor must be connected between the RT/CLK pin and the ground. This pin cannot be floated empty.

$$f_{SW}(KHz) = \frac{59500}{R_T(K\Omega)}$$

3. LDO

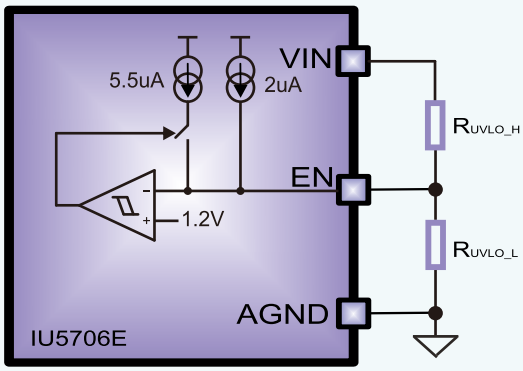
The IU5706E contains a low voltage differential regulator, which provides bias power for the controller and grid driver. The LDO output of the chip is adjusted to 6.6V. When the input voltage is lower than the VCC regulation level, the VCC output tracks the VIN voltage. The output current of VCC regulator should not exceed 50mA. The capacitance of VCC pin depends on the whole system design and its startup characteristics. The recommended range capacitance value is 0.47μF to 10μF。

4. Undervoltage Detection (UV)

The chip undervoltage detection circuit can prevent the equipment from misoperation under the input voltage lower than 3.9V (typical). When the input voltage is below the VINUV threshold, the internal PWM control circuit and the grid driver are closed. This threshold is set to 4.5V below the minimum operating voltage to ensure that the instantaneous VIN drop will not cause the chip to reset. For input voltage between UV threshold and 4.5V, the chip tries to work, but cannot ensure electrical specifications. The EN pin can be used to realize adjustable UVLO, if the expected starting threshold is higher than 3.9V. Details will be provided in the following sections.

5. Enable and Set Under Voltage Lockout (UVLO)

The EN pin voltage must be greater than 1.2V (typical) to turn on the chip. When the EN voltage is less than 0.4V, the chip enters the shutdown mode. In the shutdown mode, the input power current of the chip is less than 6μA。 EN pin has internal 2μA pull-up current source. When the EN pin is floating, the current source provides default enabling conditions. When the EN pin voltage is higher than the shutdown threshold but lower than 1.2V, the chip is in standby mode. The EN pin can be used to realize the adjustable input UVLO. As shown in the figure, use the voltage divider from VIN pin to AGND to set the UVLO level. Once the EN pin voltage exceeds 1.2V (typical) threshold voltage, the EN pin will generate an additional 5.5μA Hysteresis current. When the EN pin voltage is lower than 1.14V (typical value), the hysteresis current will be eliminated. Adding hysteresis current at the EN threshold helps to adjust the input voltage hysteresis. RUVLO_ H and RUVLO_ L is calculated as follows.



$$R_{UVLO\_H} = \frac{V_{START} * \frac{V_{EN\_DIS}}{V_{EN\_ON}} - V_{STOP}}{I_{EN\_pup} * (1 - \frac{V_{EN\_DIS}}{V_{EN\_ON}}) + I_{EN\_hys}}$$

$$R_{UVLO\_L} = \frac{R_{UVLO\_H} * V_{EN\_DIS}}{V_{STOP} - V_{EN\_DIS} + R_{UVLO\_H} * (I_{EN\_pup} + I_{EN\_hys})}$$

IU5706E Application Points

In the above formula:

- V_{START} is the preset VIN pin on voltage;
- V_{STOP} is the preset VIN pin off voltage;
- V_{EN_ON} is the EN pin enabling on voltage, 1.2V (TYP);
- V_{EN_DIS} is the EN pin enabling off voltage, 1.14V(TYP);
- I_{EN_hys} is the built-in hysteresis current of EN pin , 5.5uA(TYP);
- I_{EN_pup} is the built-in pull-up current of EN pin , 2uA(TYP);

6. Set Output Voltage

The internal reference voltage provides an accurate 1.2V voltage at the same phase end of the error amplifier. To set the output voltage, select FB pin voltage divider R_{FBH} and R_{FBL} according to the following formula.

$$V_{OUT}(V) = (\frac{R_{FBH}}{R_{FBL}} + 1) * 1.2$$

7. Soft Start

The chip has a built-in soft start circuit, which can significantly reduce the start current spike and output voltage overshoot. When the IC is enabled, the internal bias current source (typical value is 5μA) Charge the capacitor CSS on the SS pin. When the SS pin voltage is less than the internal 1.2V reference voltage, the FB pin voltage will be adjusted to the SS pin voltage instead of the internal 1.2V reference voltage. Once the SS pin voltage exceeds the reference voltage, the equipment will adjust the FB pin voltage to 1.2V. The soft start time of output voltage can be calculated by the following formula.

$$t_{ss}(mS) = \frac{1.2(V)}{5(uA)} * C_{ss}(nF)$$

8. POWER GOOD Indication

The PGOOD pin of the chip indicates whether the output voltage is within the preset range by monitoring the FB pin voltage. If this function is not used, the pin can be directly grounded or floating.

- When the output voltage is within ±10% of the set value, the PGOOD pin output is 0.
- When the output voltage is not within ±10% of the set value, the PGOOD pin output is in high resistance state. PGOOD pin can be pulled up to 24V voltage source by external resistance (10KΩ ~100KΩ recommended).

9. Output Overvoltage Protection

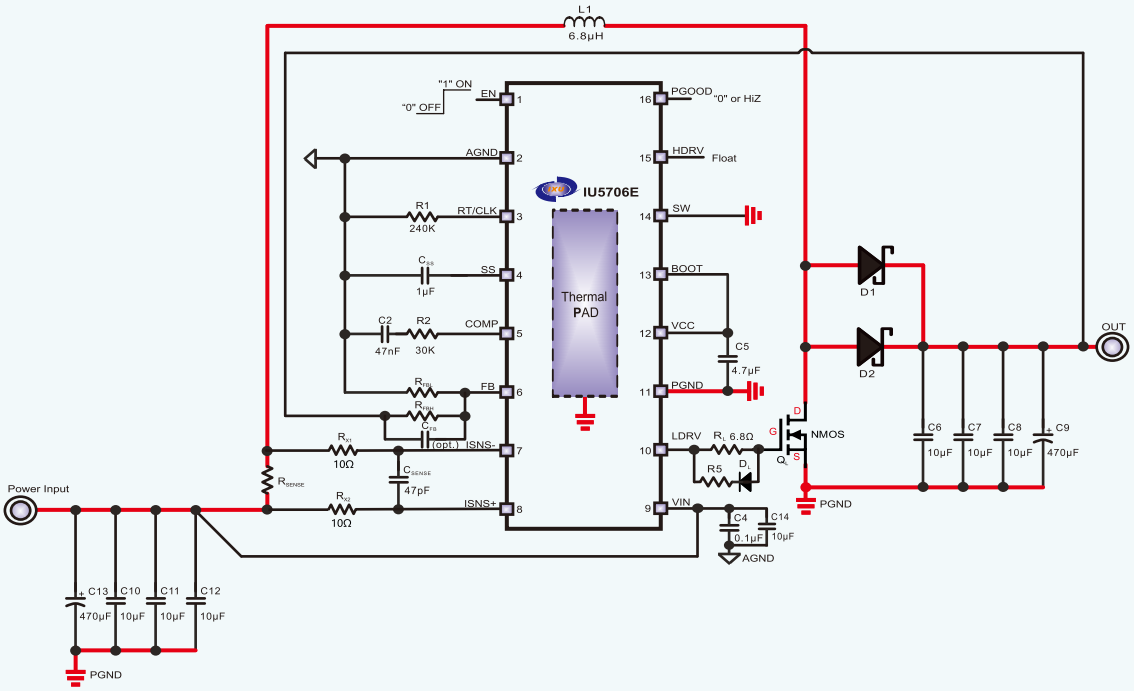
The chip integrates an overvoltage protection (OVP) circuit. When the output voltage reaches the OVP threshold (107% of the output voltage set value is fixed internally), the circuit turns off the low-side MOSFET. When the output voltage drops below 105% of the output voltage setting value, the low side MOSFET returns to normal PWM control. The OVP circuit protects the power MOSFET and minimizes the output voltage overshoot under transient or fault conditions.

10. Selection of Overcurrent Protection and Inductance Current Detection Resistance

The chip provides current limit protection cycle by cycle. When the inductive current reaches the current limit threshold, the low-side MOSFET is turned off. The current limiting circuit is reset at the beginning of the next switching cycle. During the overcurrent period, the output voltage begins to decrease with the output load. The chip has built-in slope compensation circuit to prevent sub-harmonic oscillation under high duty cycle. The slope compensation will reduce the overcurrent limit threshold (maximum current detection threshold) as the duty cycle increases. Maximum inductive current detection threshold V_{CSmax} sets the maximum peak inductive current, which is the maximum average inductive (input) current I_{ave_max} and half inductive ripple peak (ΔI_L). The detection resistance value shall be selected according to the required maximum input current and ripple current and calculated using the following formula.

$$R_{SENSE} = \frac{V_{CSmax}}{I_{ave\_max} + \frac{\Delta I_L}{2}}$$

IU5706E Asynchronous Application



IU5706E Asynchronous Application Circuit Diagram

Notes:

(1) Try to select a power inductor L1 with a small DCR, and the saturation current value must be greater than the set inductor peak current with sufficient margin.

(2)The power resistor R_{SENSE} is used to set the peak current value of the inductor, and taps must be made close to its two ends.

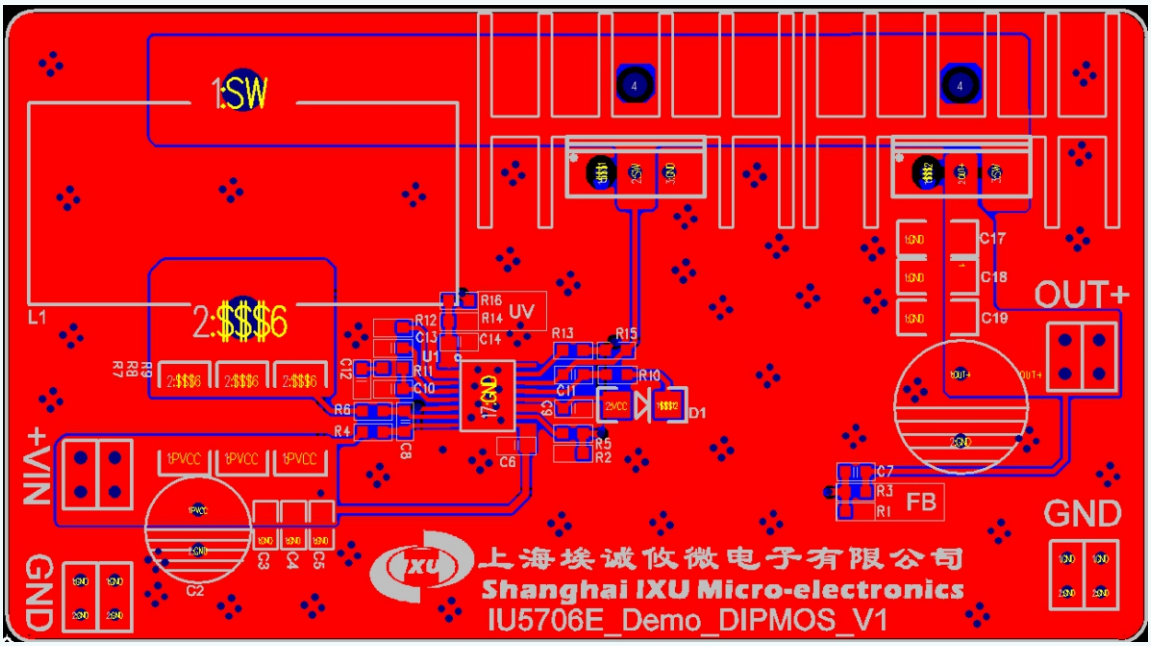
(3) The saturation current value of Schottky diodes D1 and D2 after parallel connection must be greater than the set inductor peak current with sufficient margin.

(4) A separate wire must be led from the input power supply capacitor to Pin 9 of the chip.

(5) The red solid line in the diagram indicates the large current path.

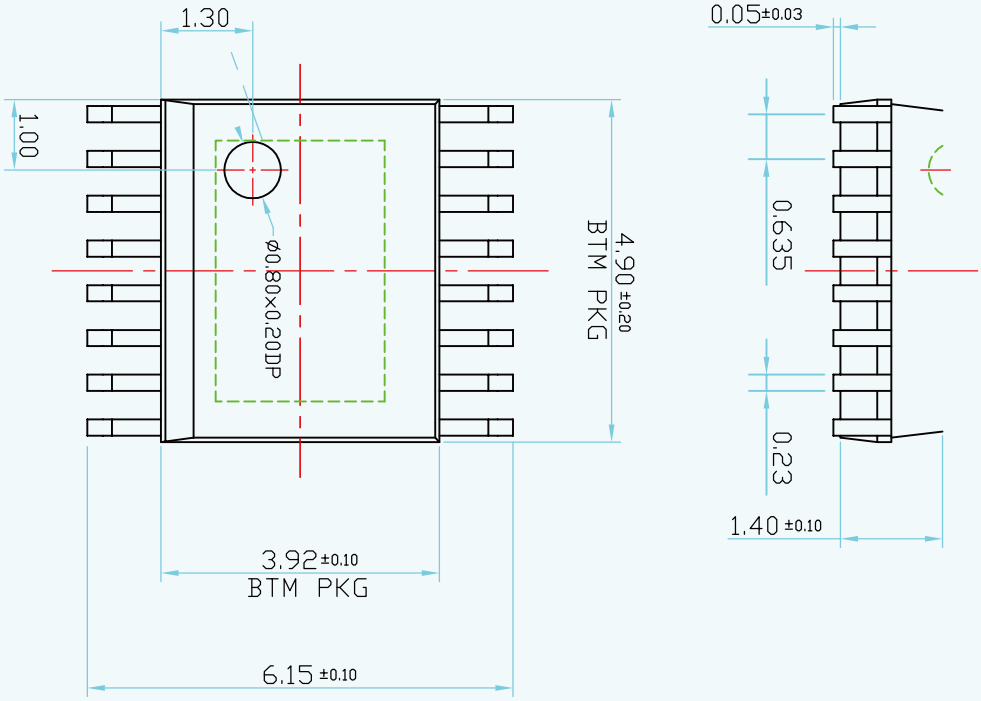
PCB Layout Recommendations

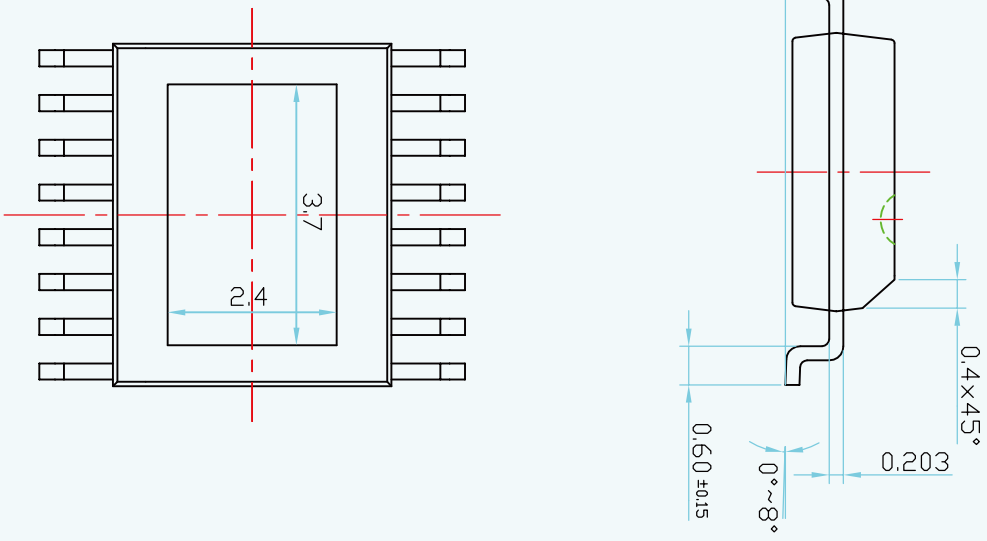
Please refer to our company's Demo layout and routing as much as possible.



Package Information

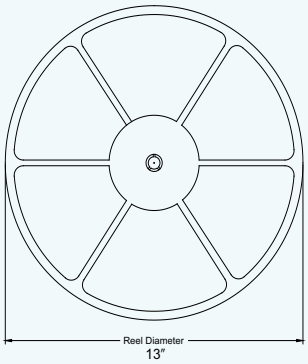
IU5706E EQA16(95*145) PACKAGE OUTLINE DIMENSIONS UNITS:MM

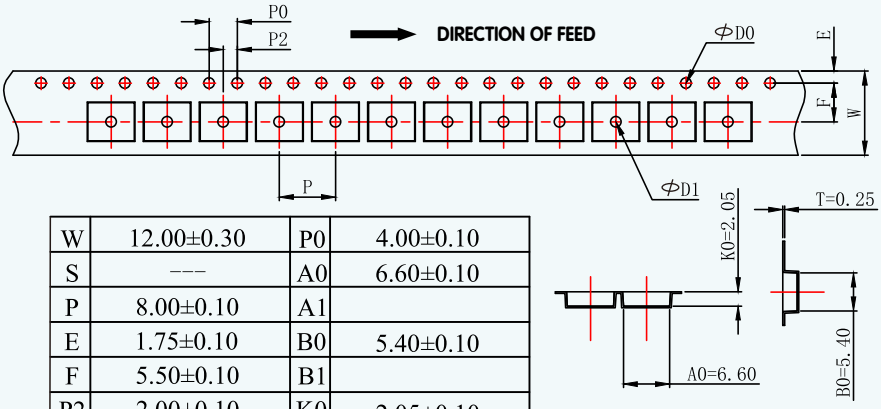




TAPE AND REEL INFORMATION

REEL DIMENSIONS





W	12.00±0.30	P0	4.00±0.10
S	---	A0	6.60±0.10
P	8.00±0.10	A1	
E	1.75±0.10	B0	5.40±0.10
F	5.50±0.10	B1	
P2	2.00±0.10	K0	2.05±0.10
D0	1.50+0.10/-0.00	K1	
D1	1.50+0.10/-0.00	t	0.25±0.05

Precautions for MOS Circuit Operation:

Static electricity can be generated in many places. The following precautions can effectively prevent MOS circuit from being damaged due to the sound of electrostatic discharge:

- Operators shall be grounded through anti-static wrist strap.
- The equipment enclosure must be grounded.
- Tools used during assembly must be grounded.
- Conductor packaging or anti-static materials must be used for packaging or transportation.

Declaration:

•Shanghai IXU Micro-electronics Co., Ltd. reserves the right to make changes to the manual without prior notice! Customers should obtain the latest version of the material before use and verify whether the relevant information is complete and up-to-date.
•Any semiconductor product has a certain possibility of failure or malfunction under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using products from Shanghai IXU Micro-electronics Co., Ltd. for system design and complete machine manufacturing, in order to avoid potential risks of failure that may cause personal injury or property damage!
•The pursuit of enhancing product quality is endless. Shanghai IXU Micro-electronics Co., Ltd. will wholeheartedly provide customers with even better products!