3.8A Brushed DC Motor Driver(PWM Control)

General Description

CS9022E is a brushed-DC motor driver suitable for printers, electrical appliances, industrial equipment, and other small machines. Two logic inputs control the H-bridge driver, which consists of four N-channel metal oxide semiconductor field-effect transistors (MOSFETs) and can bi-directional control the motor with a peak current of up to 3.8A. By utilizing the current decay mode, the motor speed can be controlled by applying pulse width modulation (PWM) to the input. If both inputs are set to low level, the motor driver will enter low power sleep mode.

CS9022E has an integrated current regulation function, which is based on the voltage of the analog input VREF and ISEN pins (proportional to the motor current flowing through the external sensing resistor). This device can limit the current to a known level, which can significantly reduce system power consumption requirements and does not require large capacitors to maintain stable voltage, especially during motor startup and shutdown. This device provides comprehensive protection against faults and short circuits, including under voltage lockout (UVLO), over current protection (OCP), and over temperature protection (TSD). After troubleshooting, the device will automatically resume normal operation.

Features

- Independent H-Bridge Motor Driver:
  Drives One DC Motor, One Winding of a Stepper Motor, or Other Loads
- Wide 6.5V to 42V Operating Voltage
- $R_{DS(on)}$ (HS+LS) : 460mΩ (Typical Value)
- 3.8A Peak Current Drive
- PWM Control Interface
- Integrated Current Regulation
- Low-Power Sleep Mode
- VM Undervoltage Lockout (UVLO)
- Overcurrent Protection (OCP)
- Thermal Shutdown (TSD)
- Automatic Fault Recovery

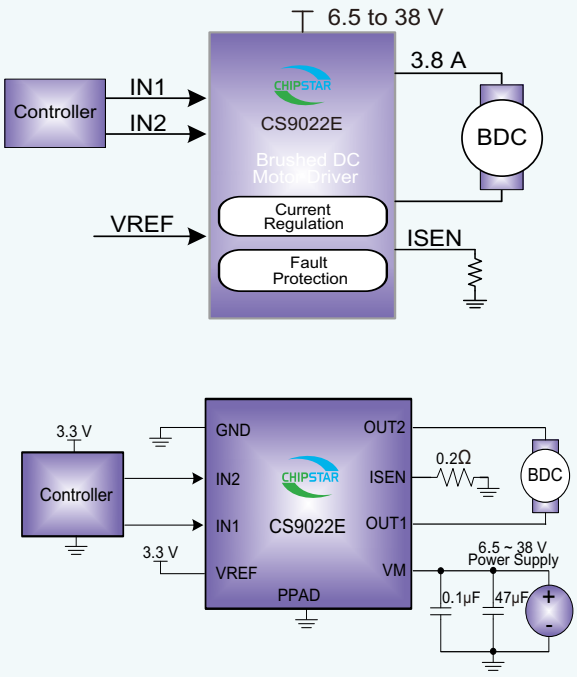
Applications

- Printers
- Appliances
- Industrial Equipment
- Other Mechatronics Applications
- Smart Home
- Sweeping robot

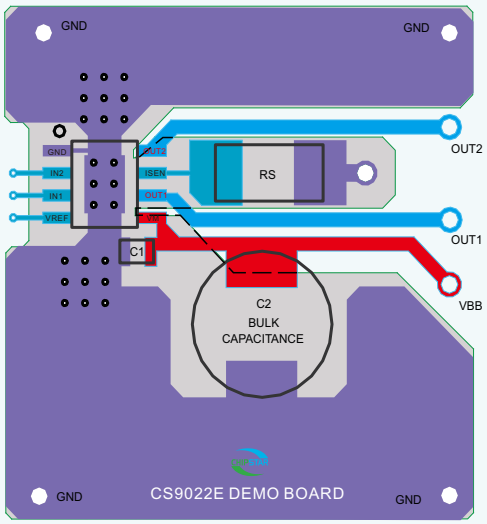
Package

- ESOP8L

Typical Applications

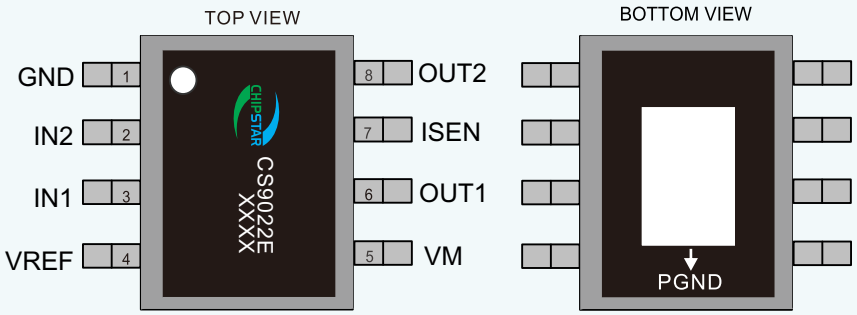


LAYOUT Recommendation



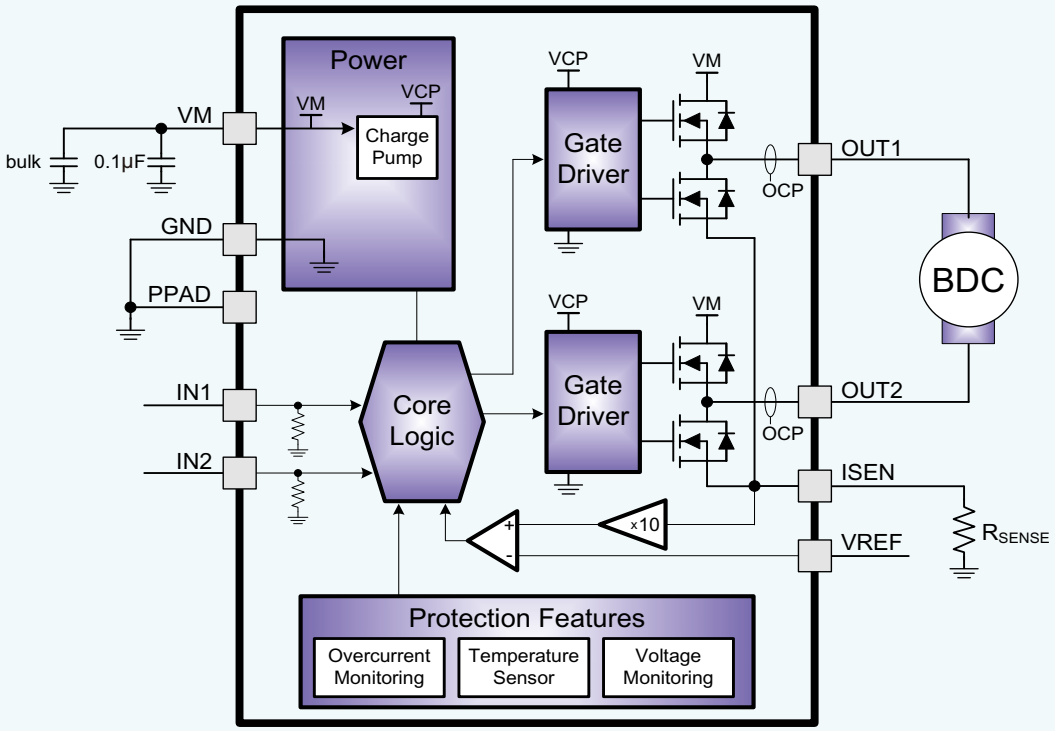
PIN Configuration and Functions

CS9022E ESOP8L



PIN		TYPE	DESCRIPTION	
NAME	NO.			
GND	1	PWR	Logic ground	Connect to board ground
IN1	3	I	Logic input	Controls the H-bridge output. Has internal pulldowns.
IN2	2			
ISEN	7	PWR	High-current ground path	If using current regulation, connect ISEN to a resistor (low-value, high-power-rating) to ground. If not using current regulation, connect ISEN directly to ground.
OUT1	6	O	H-bridge output	Connect directly to the motor or other inductive load.
OUT2	8			
PAD	9	-	Thermalpad	Connect to board ground
VM	5	PWR	6.5V~42V power supply	Connect a 0.1μF bypass capacitor to ground, as well as sufficient bulk capacitance, rated for the VM voltage.
VREF	4	I	Analog input	Reference voltage input, set driving peak current

Functional Block Diagram



Absolute Maximum Ratings [1]

SYMBOL	PARAMETER	VALUE	UNIT
VM	Power supply voltage	50	V
	Power supply voltage ramp rate	0~2	V/μs
V_{REF}	Reference input pin voltage	-0.3 to 6	V
OUT1,OUT2	Continuous phase node pin voltage	-0.7 to VM+0.7	V
IN1,IN2	Logic input voltage	-0.3 to 7	V
ISEN	Current sense input pin voltage	-0.5~1	V
T_J	Operating junction temperature	-40 to 150	℃
T_{STG}	Storage temperature	-65 to 150	℃

Recommended Operating Conditions

SYMBOL	PARAMETER	VALUE	UNIT
VM	Power supply voltage	6.5~42	V
V_I	Logic input voltage range (IN1, IN2)	0~5.5	V
I_{OUT}	Peak output current	3.8	A
f_{PWM}	Logic input PWM frequency (IN1, IN2)	<100	KHz
V_{REF}	VREF input voltage range	0.3~5.0	V
T_j	Operating junction temperature	-40~125	℃

Thermal Information [2]

SYMBOL	PARAMETER	VALUE	UNIT
θ_{JA}	Package thermal resistance - chip to environment thermal resistance	40	℃/W

Ordering Information

Device	Package Type	Device Marking	Reel Size	Tape Width	Quantity
CS9022E	ESOP8L		13''	12mm	4000 units

ESD范围

HBM (Human Body Model) ---------- ±2kV

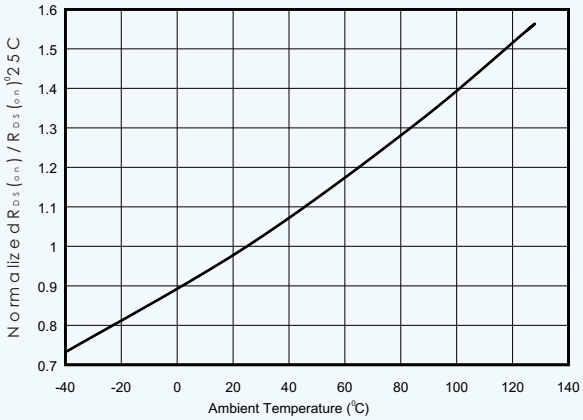
MM (Machine model) ---------- ±200V

1. The above parameters are only the limit values of device operation. It is not recommended that the working conditions of the device exceed the limit values. Otherwise, the reliability and life of the device will be affected, and even permanent damage will be caused.
2. Where the PCB board is placed in CS9022E, a heat dissipation design is needed. The heat sink at the bottom of CS9022E is connected with the heat sink area of PCB board.

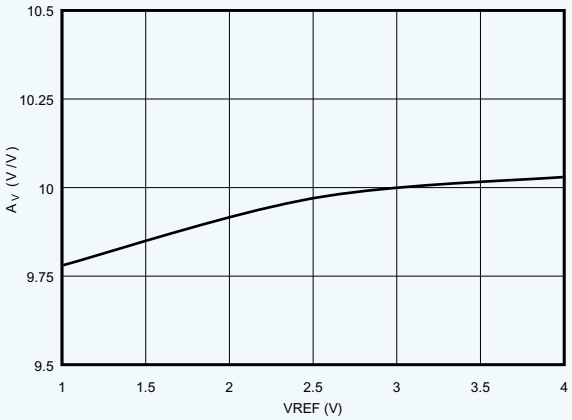
Electrical Characteristics (VM=24V，T_A=25℃，unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
I_{VM}	VM operating supply current	f_{PWM}<50kHz	3	4	10	mA
I_{VMQ}	VM sleep current	IN1=IN2=0V	9	15	20	uA
V_{UVLO}	VM undervoltage lockout	VM rising	6			V
V_{HYS}	VM undervoltage hysteresis		100	300		mV
LOGIC-LEVEL INPUTS (IN1, IN2)						
V_{IL}	Input logic low voltage			0.5	0.7	V
V_{IH}	Input logic high voltage		1.5		5.25	V
V_{HYS}	Input logic hysteresis			0.25		V
I_{IL}	Input logic low current	V_{IN}=0V	-20		20	uA
I_{IH}	Input logic high current	V_{IN}=3.3V	35		100	uA
R_{pd}	Pulldown resistance			100		kΩ
t_{DEG}	Propagation delay			450		ns
t_{SLEEP}	Time to sleep			1	1.5	ms
H-Bridge FETS						
$R_{DS(ON)}$	LS+HS on resistance	I_O=1A, T_J=25℃		460		mΩ
I_{OFF}	Output shutdown leakage current		-1		1	uA
MOTOR DRIVER						
t_{OFF}	PWM off-time			25		us
t_R	Rising time	VM=24V,22Ω to GND,10% to 90%		120		ns
t_F	Falling time	VM=24V,22Ω to GND,10% to 90%		90		ns
t_{DEAD}	Output dead time			300		ns
A_{ISEN}	ISEN gain			10		V/V
t_{BLANK}	PWM blanking time			2		us
保护电路						
I_{OCP}	Overcurrent protection trip OCP level		4.5	5	6	A
t_{OCP}	Overcurrent deglitch time			2		us
t_{RETRY}	Overcurrent retry time			3		ms
T_{SD}	Thermal shutdown temperature			150		℃
T_{HYS}	Thermal shutdown hysteresis			40		℃

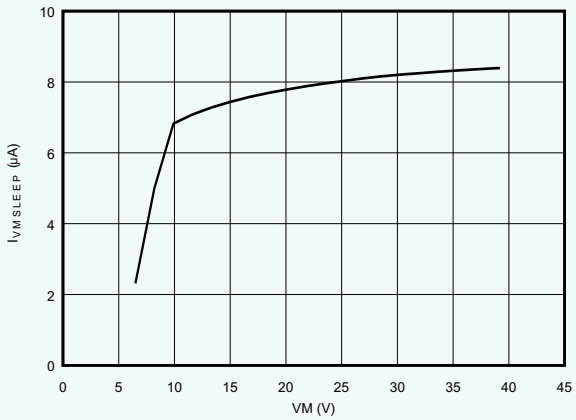
Typical Characteristics



RDS(on) vsTemperature



AV vsVREF



IVMSLEEP vs VM at 25°C

CS9022E Application Points

1. H-Bridge Control

Input pins IN1 and IN2 control the output status of the H-bridge. The following table shows the logical relationships between each other.

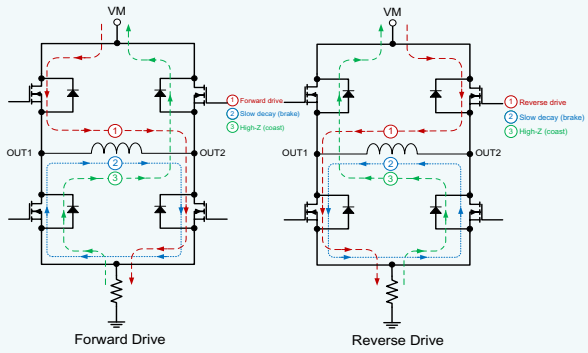
IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	Z	Z	Coast,Sleep
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake

2. PWM Control Motor Speed

The logic input can also be controlled using PWM to achieve speed regulation function. When a PWM wave is used to control a coil, when the driving current is interrupted, the inductance characteristics of the motor require the motor coil to continue flowing. In order to operate the motor coil, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, the H-bridge is turned off and the freewheeling current flows through the body diode; In slow decay mode, the two ends of the motor coil are short circuited. When PWM control is used in fast decay mode, the PWM signal controls one INx pin while the other pin maintains a low level; When used in slow attenuation, one of the pins maintains a high level.

IN1	IN2	Function
PWM	0	Forward PWM ， fast decay
1	PWM	Forward PWM ，slow decay
0	PWM	Reverse PWM ， fast decay
PWM	1	Reverse PWM ，slow decay

The following figure shows the current path under different driving and decay modes.

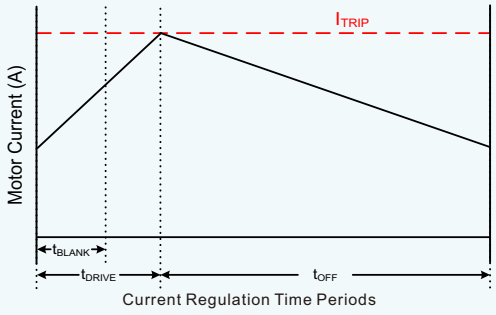


3. Current Regulation

By using a fixed frequency PWM current rectifier, the current flowing through the motor drive bridge arm is limited or controlled. In DC motor applications, the current control function is used to limit the starting current and stopping current. When an H-bridge is enabled, the current flowing through the corresponding bridge arm increases at a slope determined by the DC voltage VM and the inductance characteristics of the motor. When the current reaches the set threshold, the driver will turn off this current until the next PWM cycle begins. Note that at the moment when the current is enabled, the voltage on the ISE N pin is ignored, and after a fixed time, The current detection circuit is only enabled. This blanking time is usually fixed at 2 seconds. This blanking time also determines the minimum PWM time when the operating current decays. The PWM target current is determined by multiplying the voltage on the current detection resistor connected to the ISE N pin by a 10 times factor and a reference voltage. The reference voltage is input through VREF. The following formula calculates the target current for 100%:

$$I_{TRIP} = \frac{VREF}{A_V \times R_{ISEN}} = \frac{VREF}{10 \times R_{ISEN}}$$

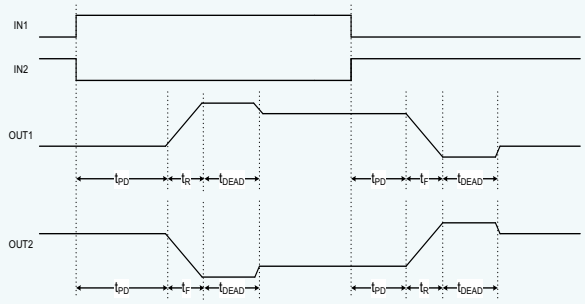
For example, if a 0.15 Ω resistor is used and the reference voltage is 3.3V, the target current is 2.2A. Note: If the current control function does not need to be used, the ISEN pin needs to be directly grounded.



When the current reaches ITRIP, the two lower tubes of the H-bridge are opened, maintained for a tOFF time (25us), and then the corresponding upper tubes are reopened.

4. Dead Time

When the output transitions from high level to low level, or from low level to high level, the existence of dead time is to prevent the upper and lower transistors from conducting simultaneously. During the dead time, the output is in a high impedance state. When it is necessary to measure the dead time on the output, it needs to be measured according to the current direction of the corresponding pin at that time. If the current flows out of this pin, the output voltage is one diode voltage drop below the ground level; If the current flows into this pin, the output voltage is one diode voltage drop higher than the power supply voltage VM.



Dead Time

5. Sleep Model

When IN1 and IN2 are both low and maintained for more than 1ms, the device will enter sleep mode, greatly reducing the idle power consumption of the device. Entering Sleep ModeAfterwards, the H-bridge of the device was disabled and the charge pump circuit stopped working. When the VM is powered on, if IN1 and IN2 are both low, the chip will enter sleep mode. When IN1 or IN2 flips to a high level and maintains at least 5us, after a delay of about 50us, the chip returns to its normal operating state.

6. Over Current Protection (OCP)

On each FET, there is an analog current limiting circuit that limits the current flowing through the FET, thereby limiting gate drive. If this over-current analog current maintains for more than the OCP pulse time, all FETs within the H-bridge are inhibited. After an OCP attempt time (t_{OCP}), the drive will be re enabled. If this error condition still exists, the above phenomenon will repeat. If this error condition disappears, the driver will resume normal operation The overcurrent conditions on the upper and lower arms of the H-bridge are independently detected. Short circuits to ground, VM, and output can all cause over-current shutdown. Note that over-current protection does not use PWM current controlled current detection circuits, so the over-current protection function does not affect the ISEN resistor.

7. Thermal shutdown Protection (TSD)

If the junction temperature exceeds the safety limit threshold, the FET of the H-bridge is prohibited. Once the junction temperature drops to a safe level, all operations will automatically return to normal. The over temperature protection circuit only protects against problems caused by high circuit temperature and should not affect the output short circuit. The threshold window size for thermal shutdown is 40℃.

8. Under Voltage Lockout Protection (UVLO)

At any time, if the voltage on the VM pin drops below the undervoltage locking threshold, all internal circuits will be inhibited and all internal resets will occur. When the voltage on the VM rises above UVLO, all functions are automatically restored.

9. Layout Considerations

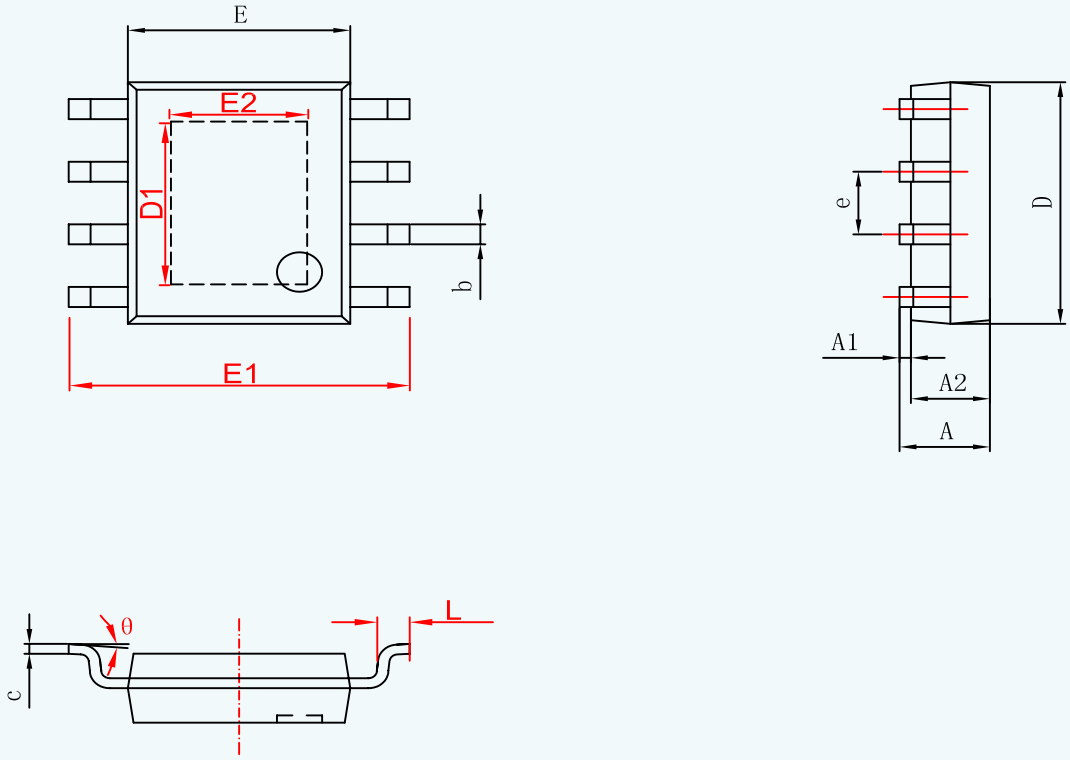
• The PCB board should be covered with large heat dissipation fins, and the connection of the ground wire should have a wide ground wire cover. In order to optimize the electrical and thermal performance of the circuit, the chip should be directly attached to the heat sink. For the electrode power supply VM, an electrolytic capacitor of not less than 47uF should be connected for ground coupling, and the capacitor should be placed as close to the device as possible. In order to avoid capacitance coupling problems caused by high-speed dv/dt conversion, the output circuit wiring of the driving circuit should be far away from the logic control input circuit wiring. The leads at the logic control end should be routed with low impedance to reduce noise caused by thermal resistance.

• A star shaped divergent ground wire overlay located under the device will be an optimized design. Adding a copper heat sink below the covered ground wire will better optimize circuit performance.

• In order to reduce errors caused by parasitic resistance on the ground wire, the ground wire of the sampling resistor R_{ISEN} should be set separately, and the ground wire should be as short and thick as possible, so that the resistance value of the parasitic resistance is much smaller than R_{ISEN}. Try to avoid using test adapter sockets for PCB boards. The connection resistance of the test sockets may also change the R_{ISEN} value, causing a deviation in the current setting.

Package Information

CS9022E ESOP8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Notes:
(1) All dimensions are in mm
(2) Refer to JEDEC mo-187 standard