Low No-Load Current, AM Suppression Function 2X150W Stereo Class D Audio Power Amplifier

General Description

CS8736E is a 2X150W stereo Class D audio amplifier. This device features a thermal pad designed on the top layer. When a heat sink is connected to the pad, it can achieve a continuous power output of over 2X150W and can drive loads as low as 2Ω under appropriate power supply voltage.

The chip incorporates advanced EMI suppression technology. It adopts surface-mount technology and requires only a small number of peripheral components to enable the system to deliver high-quality audio output power.

The CS8736E integrates over-current protection, short-circuit protection, and over-temperature protection, effectively preventing the chip from being damaged under abnormal operating conditions. With a maximum efficiency of over 92% and a voltage tolerance design of over 45V, the CS8736E offers ultra-high reliability, which can effectively reduce the defect rate during production.

The CS8736E provides a special EFB40 package option for customers. The appropriate package size maximizes convenience for customers to install heat dissipation components, and its rated operating temperature range is -20℃ to 85℃.

Features

- Output Power (THD+N = 10%)
  VDD = 24V @ RL = 4Ω: 2X80W
  VDD = 28V @ RL = 4Ω: 2X110W
  VDD = 30V @ RL = 4Ω: 2X130W
  VDD = 32V @ RL = 4Ω: 2X140W
  VDD = 34V @ RL = 4Ω: 2X155W
  VDD = 36V @ RL = 8Ω: 2X99W
- Wide Voltage Range Single Power Supply: 5V~36V
- High-Reliability Design: 45V Voltage Tolerance Design
- Efficiency: 92%@PVCC = 15V, PO = 2X20W
- Three Selectable Gain Levels
- Mute function control
- Quiescent Current: 30mA@24V with Filter Network
- Multiple Selectable Switching Frequencies: AM Suppression Frequency Selection Function
- Output Pins Facilitating Wiring and Layout
- Excellent Short-Circuit Protection and Temperature Protection with Auto-Recovery Function
- Excellent Distortion Performance and Pop Noise Prevention
- Differential Input
- Enhanced Package Design: Special Design of Top-Layer Thermal Pad
- Compliant with Automotive Application Requirements

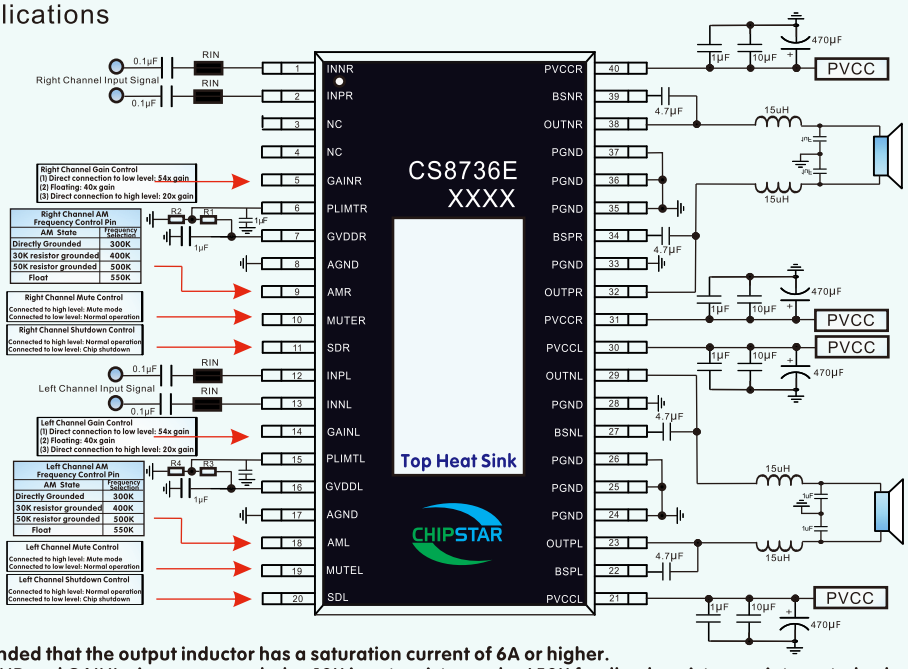
Applications

- Automotive Audio
- Home Audio System
- Emergency Call

Package

- EFB40

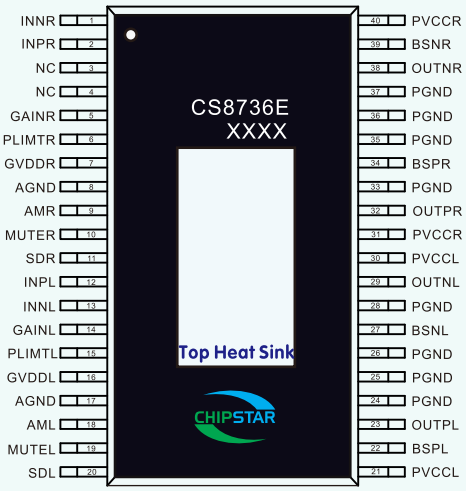
Typical Applications



Notes:

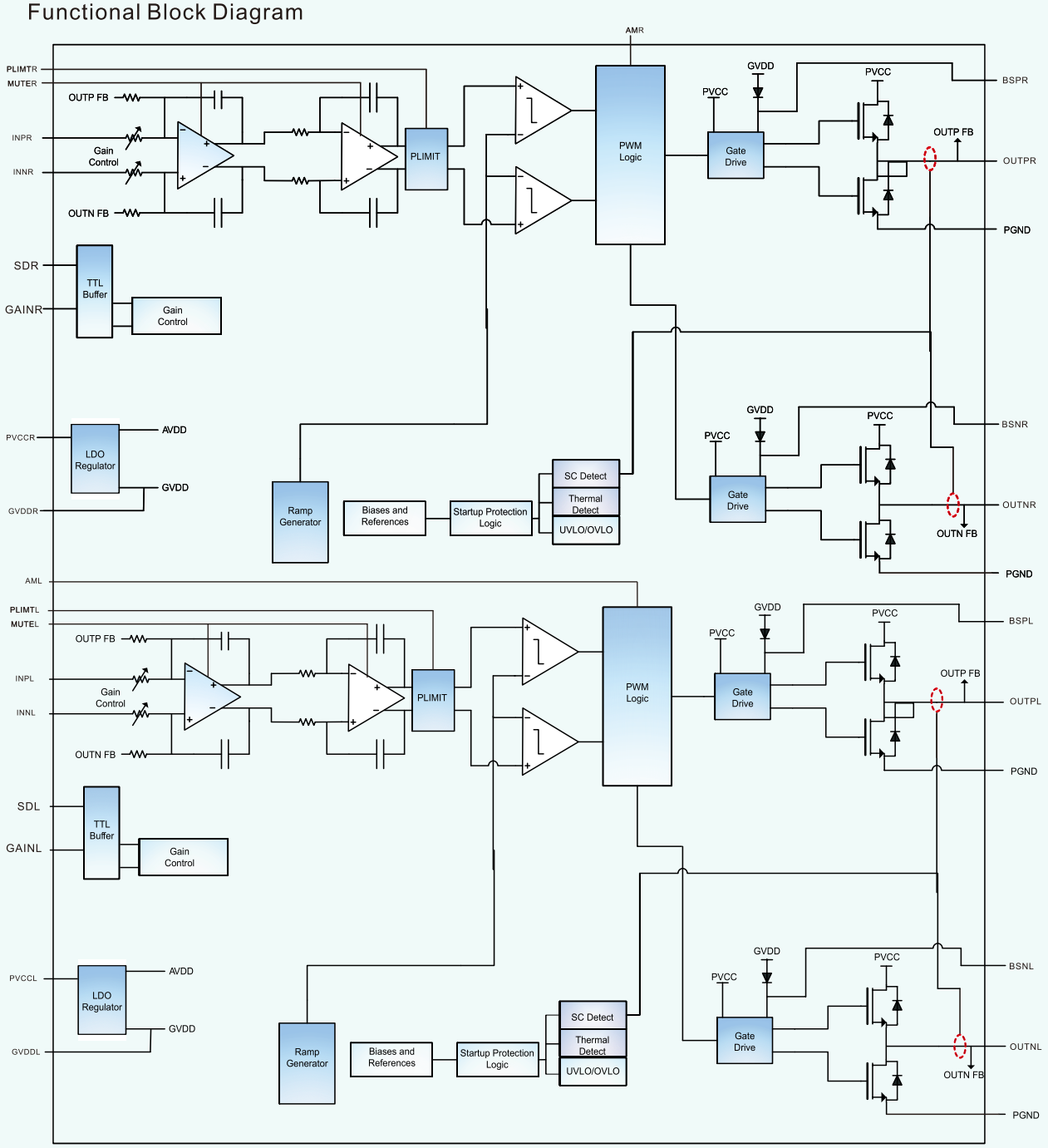
- **It is recommended that the output inductor has a saturation current of 6A or higher.**
- **When the GAINR and GAINL pins are grounded, a 12K input resistor and a 650K feedback resistor are integrated; when the GAIN pin is floating, a 15.2K input resistor and a 610K feedback resistor are integrated; when the GAIN pin is connected to a high level, a 25.5K input resistor and a 510K feedback resistor are integrated.**
- **If AMR and AML need to be connected together to select the switching frequency, the corresponding resistor to ground must be halved.**

PIN Configuration and Functions



NO.	NAME	I/O	DESCRIPTION	NO.	NAME	I/O	DESCRIPTION
1	INNR	I	Right Channel Audio Input Negative Terminal	21	PVCCL	P	Left Channel Power Supply
2	INPR		Right Channel Audio Input Positive Terminal	22	BSPL	I	Left Channel Positive Output Upper Transistor Bootstrap
3	NC	-	Unused Pin	23	OUTPL	O	Left Channel Audio Output Positive Terminal
4	NC	-	Unused Pin	24	PGND	-	Power Ground
5	GAINR	I	Right Channel Gain Control Pin	25	PGND	-	Power Ground
6	PLIMTR	I	Right Channel Power Output Limitation Pin	26	PGND	-	Power Ground
7	GVDDR	I	Right Channel Upper Transistor Gate Drive Voltage	27	BSNL	I	Left Channel Negative Output Upper Transistor Bootstrap
8	AGND	-	Analog Ground	28	PGND	-	Power Ground
9	AMR	I	Right Channel AM Frequency Control Pin	29	OUTNL	O	Left Channel Audio Output Negative Terminal
10	MUTER	I	Right Channel Mute Control Pin	30	PVCCL	P	Left Channel Power Supply
11	SDR	I	Right Channel Shutdown Control Pin	31	PVCCR	P	Right Channel Power Supply
12	INPL	I	Left Channel Audio Input Positive Terminal	32	OUTPR	O	Right Channel Audio Output Positive Terminal
13	INNL	I	Left Channel Audio Input Negative Terminal	33	PGND	-	Power Ground
14	GAINL	I	Left Channel Gain Control Pin	34	BSPR	I	Right Channel Positive Output Upper Transistor Bootstrap
15	PLIMTL	I	Left Channel Power Output Limitation Pin	35	PGND	-	Power Ground
16	GVDDL	I	Left Channel Upper Transistor Gate Drive Voltage	36	PGND	-	Power Ground
17	AGND	-	Analog Ground	37	PGND	-	Power Ground
18	AML	I	Left Channel AM Frequency Control Pin	38	OUTNR	O	Right Channel Audio Output Negative Terminal
19	MUTEL	I	Left Channel Mute Control Pin	39	BSNR	I	Right Channel Negative Output Upper Transistor Bootstrap
20	SDL	I	Left Channel Shutdown Control Pin	40	PVCCR	P	Right Channel Power Supply

Functional Block Diagram



Absolute Maximum Ratings[1]

			VALUE
V_{CC}	Power Supply	PVCC	-0.3V to 45V
V_I	Input Pin Voltage	SDR,SDL	-0.3V to 45V
		GAINR,GAINL,PLIMTR,PLIMTL INNR,INPR,INPL,INNL MUTER,MUTEL,AMR,AML	-0.3V to 6.0V
T_A	Operating Temperature Range		-40℃ to 85℃
T_J	Junction Operating Temperature Range		-40℃ to 150℃
T_{stg}	Storage Temperature Range		-40℃ to 150℃

Recommended Operating Environment

SYMBOL	PARAMETER	VALUE	UNIT
PV_{CC}	Input power supply voltage	5~36	V
T_J	Junction operating temperature range	-40~125	℃
T_A	Ambient temperature range	-40~85	℃

Thermal Information

SYMBOL	PARAMETER	VALUE	UNIT
θ_{JA}	Package thermal resistance - chip to environment thermal resistance	12	℃/W
θ_{JC}	Package thermal resistance - chip to Package Surface thermal resistance	5	℃/W

Ordering Information

Device	Package Name	Device Marking	Package Type	Quantity
CS8736E	EFB40		Tube	36

ESD Ratings

HBM (Human Body Model) ---------- ±2KV

MM (Machine model) ---------- ±200V

1. The above parameters are merely the limit values for the device's operation. It is not recommended to operate the device beyond these limits; otherwise, it will affect the device's reliability and service life, and may even cause permanent damage.

Recommended Operating Conditions

			MIN	MAX	UNITS
V_{CC}	Power Supply	PVCCR,PVCCL	5	36	V
V_{IH}	Input High Level	SD(R,L),MUTE(R,L),AM(R,L),PLIMT(R,L),GAIN(R,L)	2		V
V_{IL}	Input Low Level	SD(R,L),MUTE(R,L),AM(R,L),PLIMT(R,L),GAIN(R,L)		0.2	V
I_{IH}	High-Level Input Current	SD(R,L),MUTE(R,L),AM(R,L),PLIMT(R,L),GAIN(R,L),VI=2V,PVCC=20V		50	uA
I_{IL}	Low-Level Input Current	SD(R,L),MUTE(R,L),AM(R,L),PLIMT(R,L),GAIN(R,L),,VI=0.2V,VCC=20V		5	uA
OVP	Overvoltage Protection			45	V

DC Parameters

Description		Test Conditions		MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output Offset Voltage	V_{IN}=0V，GAIN=36dB			6	15	mV
I_{CC}	Quiescent Current	SD(R,L)=2V,4Ω speaker ,PV_{CC}(R,L) =18V			30	40	mA
$I_{CC(SD)}$	Standby Current	SD=0V,No Load and No Filter,PV_{CC}=24V			100	600	uA
$r_{DS(on)}$	Drain-Source On-Resistance	V_{CC} =21V,I_O=500mA, T_J =25℃	Upper Transistor		100		mΩ
			Lower Transistor		100		
t_{on}	Turn-On Time	SD=2V			210		ms
t_{OFF}	Turn-Off Time	SD=0V			2		us
GVDD	Gate Drive Voltage	I_{GVDD} =100 mA		4.25	4.75	5.25	V
Vo	Maximum Output Voltage Under Power Limitation	$V_{(PLIMIT)}$ = 2V; V_I = 1Vrms			6.5		V
f_{OSC}	Oscillation Frequency	AM Directly grounded		270	300	330	KHz
		AM 30KΩ grounded		360	400	440	
		AM 50KΩ grounded		450	500	550	
		AM Float		500	550	600	

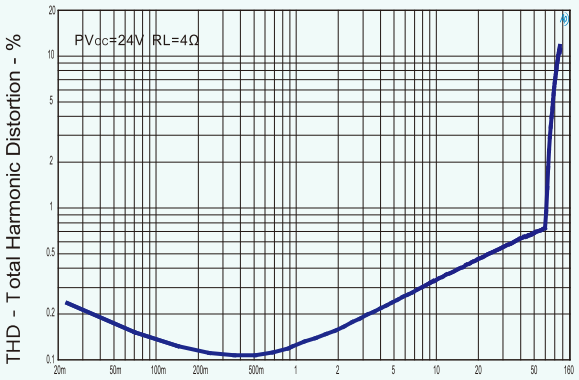
AC Parameters

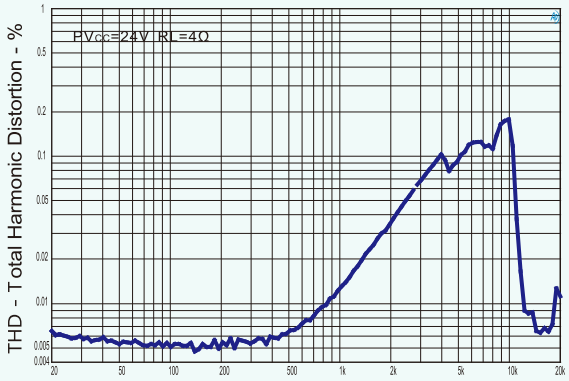
Description		Test Conditions	MIN	TYP	MAX	UNIT
K_{SVR}	Power Supply Rejection Ratio	1kHz，200mVpp Ripple，Gain=20dB Input AC-Coupled to Ground		70		dB
THD+N	Total Harmonic Distortion plus Noise	PV_{CC}=24V， f=1kHz, Po=20W		0.05		%
	Output Noise	20~22kHz， Aweight，Gain=20dB		100		uV
				-78		dBV
	Efficiency	PV_{CC}=15V， f=1kHz, Po=20W		92		%
SNR	Signal-to-Noise Ratio	Maximum Output at Gain = 20dB，THD+N < 1%，f=1kHz		102		dB
	Thermal Protection Temperature			170		℃
	Hysteresis Temperature			15		℃

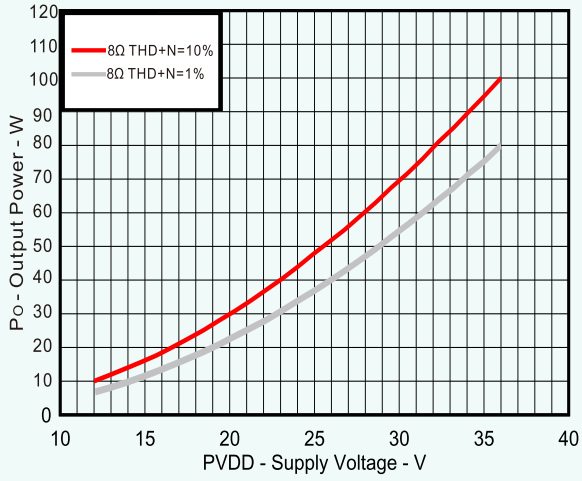
Po	Output Power	V_{DD} = 24V@RL = 4 Ω	THD+N=10%@P_O=80W	THD+N=1%@P_O=64W
		V_{DD} = 24V@RL = 2 Ω	THD+N=1%@P_O=2X105W	
		V_{DD} = 28V@RL = 4 Ω	THD+N=10%@P_O=2X108W	THD+N=1%@P_O=2X88W
		V_{DD} = 28V@RL = 3 Ω	THD+N=10%@P_O=2X140W	THD+N=1%@P_O=2X115W
		V_{DD} = 30V@RL = 4 Ω	THD+N=10%@P_O=2X130W	THD+N=1%@P_O=2X106W
		V_{DD} = 32V@RL = 4 Ω	THD+N=10%@P_O=2X140W	THD+N=1%@P_O=2X115W
		V_{DD} = 34V@RL = 4 Ω	THD+N=10%@P_O=2X155W	THD+N=1%@P_O=2X126W
		V_{DD} = 36V@RL = 8 Ω	THD+N=10%@P_O=2X99W	THD+N=1%@P_O=2X80W

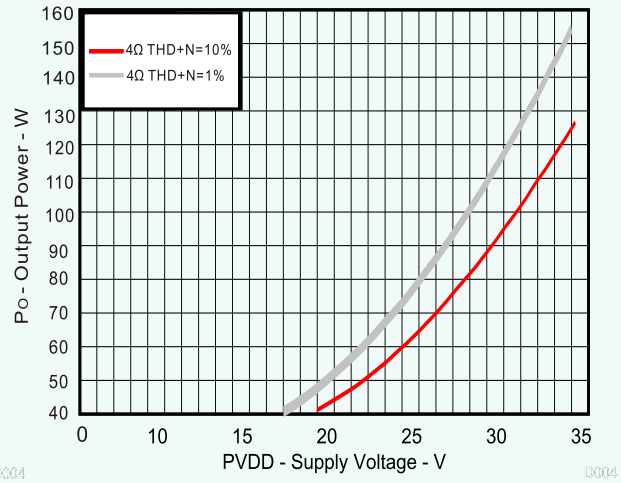
TYPICAL PERFORMANCE CHARACTERISTICS

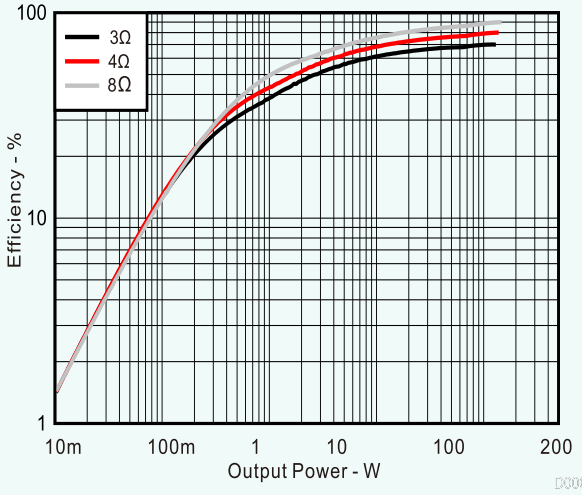
All tests are based on a 1KHz signal (unless otherwise specified)



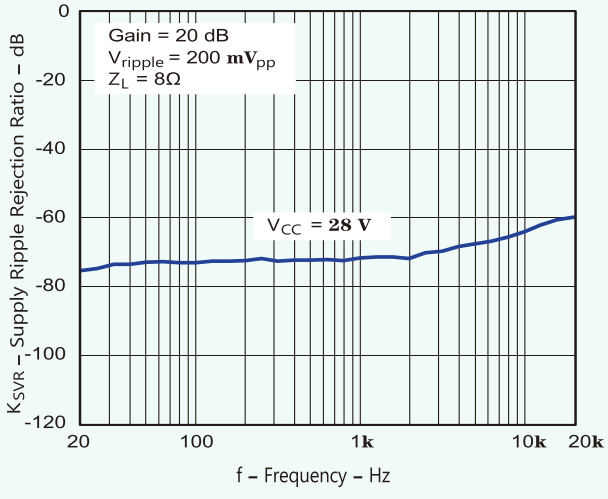








Efficiency vs Output Power



SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

CS8736E Application Points

Gain Setting

The CS8736E is equipped with gain control pins GAINR and GAINL. The table below outlines the gain control methods of the CS8736E, along with the corresponding integrated input and feedback resistor values.

GAINR,GAINL	Amplification Factor	Input Resistor	Feedback Resistor
Connected directly to low level	54X	12K	650K
Float	40X	15.2K	610K
Connected directly to high level	20X	25.5K	510K

Short-Circuit Protection and Automatic Recovery

The CS8736E provides protection against overcurrent conditions caused by output short circuits. When a short circuit occurs, the CS8736E immediately shuts down the output. After the output short-circuit fault is resolved, the CS8736E will automatically recover after a 110ms waiting period.

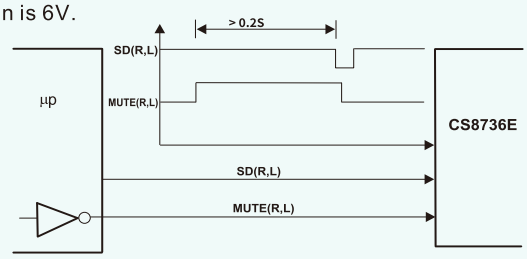
Temperature Protection

The temperature protection function of the CS8736E prevents device damage when the temperature exceeds 170°C. There is an allowable range of ±15°C among devices at this temperature point. Once the temperature exceeds the set temperature point, the device enters a shutdown state with no output. When the temperature drops by 20°C, the temperature protection is cleared, and the device resumes normal operation.

Mute Function and Shutdown Control

The SDR and SDL input pins should be at a high potential when the CS8736E is operating normally. When the SD pin is pulled to a low potential, the output is turned off, and the circuit enters standby mode. The maximum voltage that can be applied to the SD pin is PVCC.

The MUTE input pin should be at a low potential when the CS8736E is operating normally. When the MUTE pin is pulled to a high potential, the output stage of the CS8736E is turned off, and the CS8736E enters mute mode. The maximum withstand voltage of the MUTE pin is 6V.



AM Suppression Function

The CS8736E enables the selection of MOS switching frequency through the control of the AMR and AML pins, as shown in the table below:

AMR,AML	Frequency Selection
Directly Grounded	300K
30K resistor grounded	400K
50K resistor grounded	500K
Float	550K

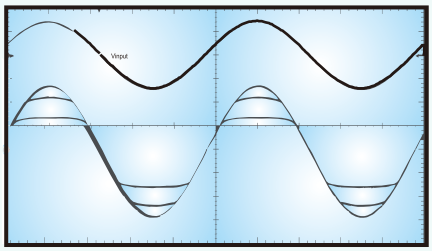
Power Limitation

The principle of the power limitation function is to restrict the maximum duty cycle of the PWM (Pulse-Width Modulation) output from the power amplifier, thereby limiting the maximum output power. Users can control the value of the maximum duty cycle by setting the voltage on the PLIMIT pin, which in turn determines the set value of the maximum power.

The power limitation method that restricts the maximum duty cycle produces a result similar to reducing the PVCC supply voltage: the output waveform is a distorted clipping waveform, as shown in the figure. During power limitation, if the input analog signal increases further, the distortion of the output waveform will increase, and the power will rise slowly.

Voltage divider resistors can be added between GVDDR, GVDDL and ground to set the voltages of PLIMITR and PLIMITL, which are used to limit the output power. The higher the voltage divided by PLIMITR and PLIMITL, the greater the allowable output power. A 1μF capacitor should be added between PLIMITR, PLIMITL and ground.

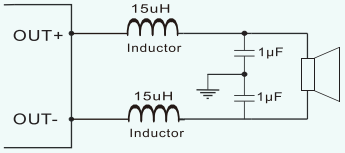
If the power limitation function is not required, PLIMITR and PLIMITL can be directly connected to the GVDDR and GVDDL pins.



CS8736E Power Limitation Waveform

Inductor and Capacitor

The CS8736E requires an inductor and a filter capacitor to be connected to its output terminal. It is recommended that the inductor used has a saturation current of 6A or higher during operation. The specific parameters are shown in the figure below:



CS8736E PCB Design Guide

To enhance the design reliability of the audio system, please pay special attention to the following points when designing the PCB layout for the CS8736E:

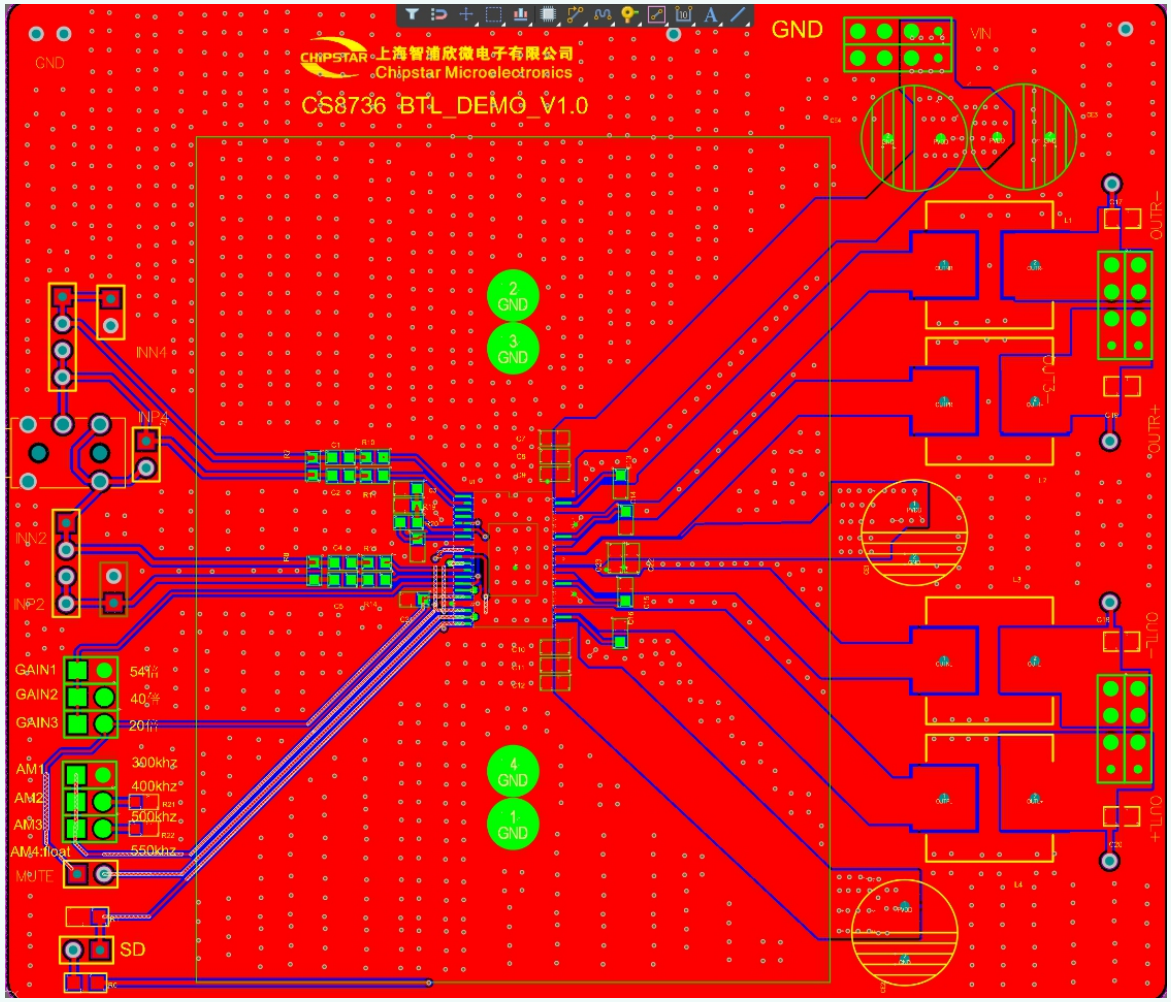
The high-current path of the chip is: VIN → chip PVCC → GND. The routing rules for the high-current path are to be as short and thick as possible, with exposed copper and additional soldering to reduce the impedance caused by PCB traces.

For the power supply pins of the CS8736E, two ceramic capacitors (10μF and 1μF) must be mounted as close as possible to the chip pins. It is recommended to use a 470μF electrolytic capacitor for the power supply pin.

All GNDs, including those of each capacitor, should be well connected. They can be connected to the large-area GND copper foil nearby to minimize the ground loop impedance and inductive reactance.

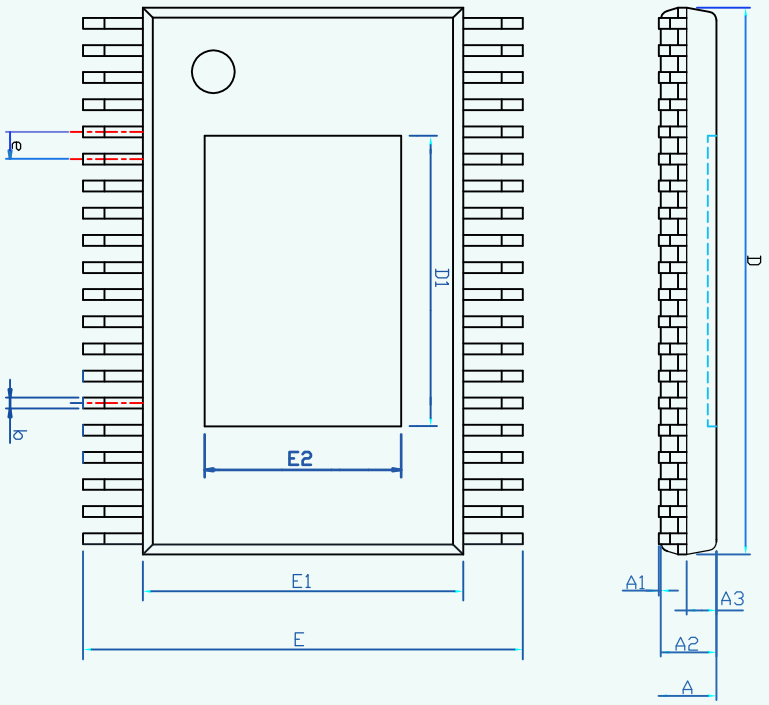
In addition, the heat sink for the Demo Board is recommended to be a high-density toothed heat sink with dimensions (length × width × height) of 60mm × 80mm × 26mm.

The following is a demo example image:

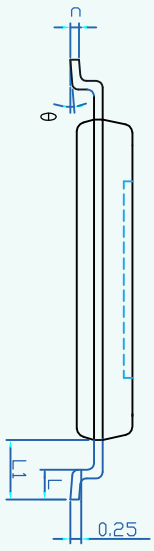


Package Information

CS8736E EFB40 Package Outline Dimensions units:mm



SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	-	-	1.43
A1	0.02	0.05	0.08
A2	1.20	1.30	1.40
A3	0.65	0.70	0.75
b	0.20	--	0.30
c	0.20	--	0.24
D	12.70	12.80	12.90
D1	6.80REF		
e	0.635 BSC		
E	10.25	10.35	10.45
E1	7.40	7.50	7.60
E2	4.60REF		
L	0.55	0.70	0.85
L1	1.40REF		
θ	0°	-	8°



Precautions for MOS Circuit Operation:

Static electricity can be generated in many places. The following precautions can effectively prevent MOS circuit from being damaged due to the sound of electrostatic discharge:

- Operators shall be grounded through anti-static wrist strap.
- The equipment enclosure must be grounded.
- Tools used during assembly must be grounded.
- Conductor packaging or anti-static materials must be used for packaging or transportation.

Declaration:

- Chipstar Micro-electronics Co., Ltd. reserves the right to make changes to the manual without prior notice! Customers should obtain the latest version of the material before use and verify whether the relevant information is complete and up-to-date.
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