40W Filter-Free MONO ClassD Audio Power Amplifier

FEATURES

- PO= 12.5W RL=2Ω @THD+N=10% VDD=7.4V
- PO= 18W RL=2Ω @THD+N=10% VDD=9V
- PO= 20W RL=4Ω @THD+N=10% VDD=12V
- PO= 23.5W RL=3Ω @THD+N=10% VDD=12V
- PO= 32W RL=4Ω @THD+N=10% VDD=16V
- PO= 40W RL=4Ω @THD+N=10% VDD=18V
- 92% Efficient ClassD Operation into 8Ω Load Eliminates Need for Heat Sinks
- Supply Voltage Range: Operation from4.5 to 23V
- Filter-Free Operation
- Flow Through Pin Out Facilitates Easy Board Layout
- Robust Pin-to-Pin Short Circuit Protection and Thermal Protection with Auto-Recovery Option
- Excellent THD+N/ Pop Free Performance
- Four Selectable, Fixed Gain Settings
- Differential Inputs

APPLICATIONS

- Televisions

DESCRIPTION

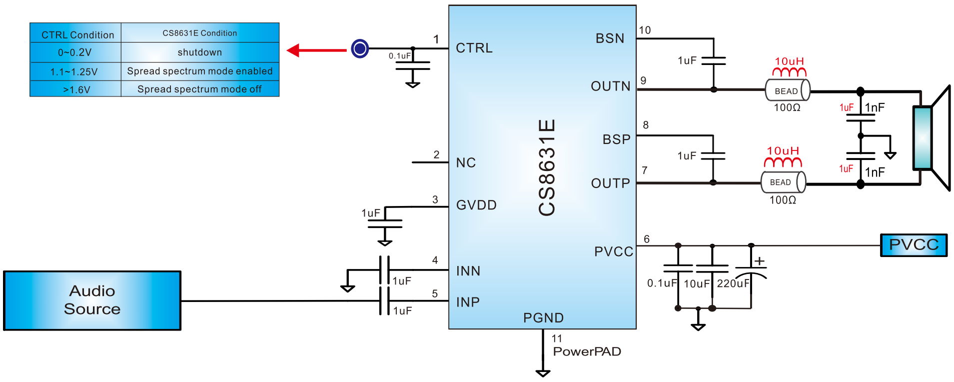
The CS8631E is a 32W efficient, ClassD audio power amplifier for driving a bridge tied speaker.Advanced EMI Suppression Technology enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements. SpeakerGuard™ speaker protection system includes an adjustable power limiter. The adjustable power limiter allows the user to set a "virtual" voltage rail lower than the chip supply to limit the amount of current through the speaker.

The CS8631E can drive a mono speaker as low as 4Ω. The high efficiency of the CS8631E > 92%,eliminates the need for an external heat sink when playing music. The outputs are fully protected against shorts to GND, VCC, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

Package

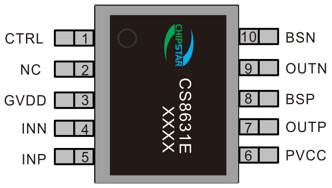
ESOP10

Typical Application

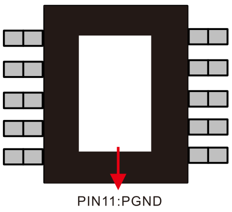


CTRL Condition	CS8631E Condition
0~0.2V	shutdown
1.1~1.25V	Spread spectrum mode enabled
>1.6V	Spread spectrum mode off

Pin Descriptions



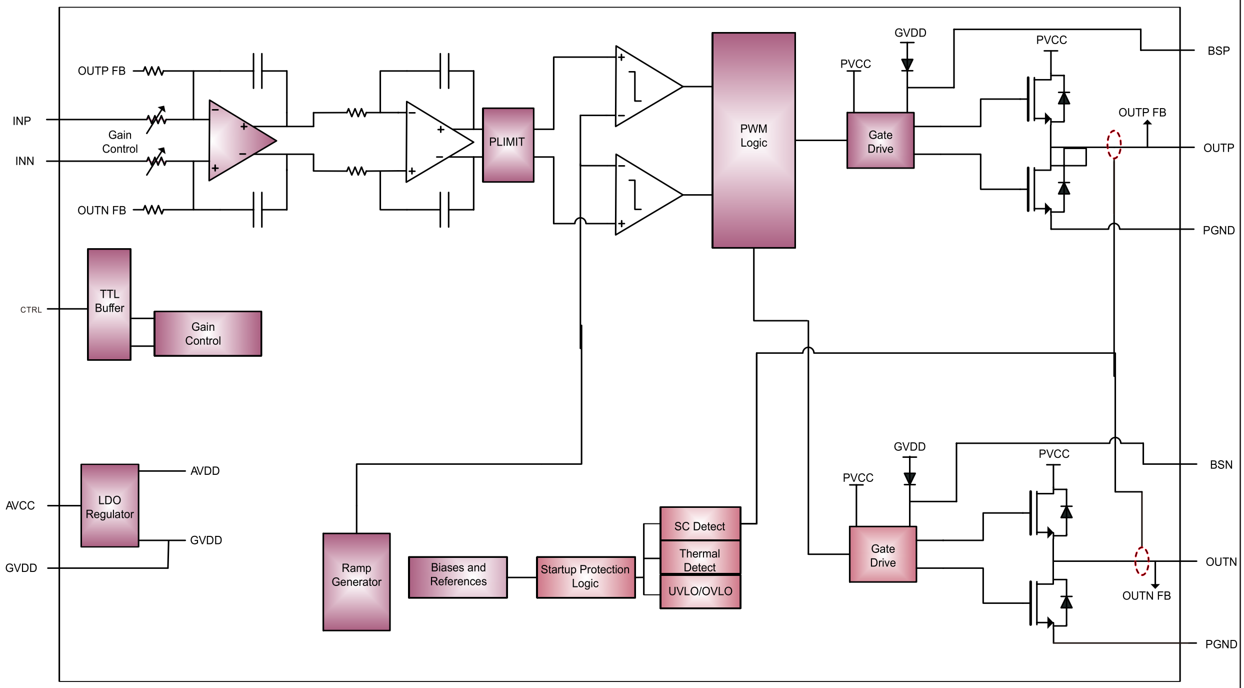
TOP VIEW



BOTTOM VIEW

NO	NAME	I/O	DESCRIPTION
1	/SD	I	SD/Spread spectrum logic input for audio amp
2	NC	—	NC
3	GVDD	P	High-side FET gate drive supply.
4	INN	I	Negative audio input
5	INP	I	Positive audio input
6	PVCC	P	Power supply
7	OUTP	O	Class-D H-bridge positive output
8	BSP	I	Bootstrap I/O, positive high-side FET.
9	OUTN	O	Class-D H-bridge negative output.
10	BSN	I	Bootstrap I/O , negative high-side FET.
11	PGND	GND	Power ground for the H-bridges.

Block Diagram



over operating free-air temperature range(unless otherwise noted)(1)

			单位
V_{CC}	Supply voltage	PVCC	0.3Vto24V
V_I	Interface pin voltage	CTRL	0.3VtoV$_{CC}$+0.3V
		INN,INP	0.3Vto18V
T_A	Operating free-air temperature range		-40℃ to 85℃
T_J	Operating junction temperature range		-40℃to150℃
T_{stg}	Storage temperature range		-65℃ to150℃
R_L	Load	BTL:PVCC>15V	4.8
		BTL:PVCC ≤15V	3.2

Thermal information[2]

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	45	℃/W
θ_{JC}	Junction-to-case (top) thermal resistance	10	℃/W
θ_{JB}	Junction-to-board thermal resistance	17.5	℃/W

Order Information

Device	Package	Making	Reel Size	Tape Width	Quantity
CS8631E	ESOP10L		Tube		100

ESD Range

ESD HBM mode -- ±2kV
ESD MM mode -- ±200V

1,The ThermalPad on the bottom of the IC should soldered directly to the PCB's ThermalPad area that with several thermal vias connect to the ground plan,and the PCB is a 2-layer,5-inch square area with 2oz copper thickness.
2,Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device.Functional operation at conditions other than the operating conditions specified is not implied.Only one Absolute Maximum Rating should be applied at one time.

Recommended Operating Conditions

PARAMETER	TEST CONDITIONS	Min	Max	Unit
V_{CC} Supply voltage	PVCC,AVCC	4.5	23.0	V
V_{IH} “H” input voltage	$\overline{SD}$	2		V
V_{IL} “L” input voltage	$\overline{SD}$		0.8	V
V_{OL} “H” output voltage	$R_{PULL-UP}$ =100k,V_{CC} =15V		0.8	V
I_{IH} “H” input current	$\overline{SD}$,V_I =2V,V_{CC}=15V		50	uA
I_{IL} “L” input current	$\overline{SD}$,V_I=0.8V,V_{CC}=15V		5	uA

DC CHARACTERISTICS T_A = 25℃, V_{CC} = 12 V, RL = 8 Ω (unless otherwise noted)

PARAMETER	TEST CONDITIONS		Min	Typ	Max	Uuit
$\|V_{OS}\|$ Offset Voltage	V_I =0V,Gain=36dB			1.5	15	mV
I_{CC} Quiescent supply current	CTRL=2.0V,no load,PV_{CC}=12V			6.5	9.0	mA
$I_{CC(SD)}$ Quiescent supply current in sd mode	CTRL=0.8V,no load,PV_{CC}=12V			20	50	uA
$r_{DS(on)}$ Drain-source on-state resistance	V_{CC} =12V,I_O=500mA, T_J =25℃	High Side		80		mΩ
		Low side		80		
t_{on} Turn-on time	CTRL=2.0V			180		ms
t_{OFF} Turn-off time	CTRL=0.8V			2		us
GVDD Gate Drive Supply	I_{GVDD} =100 mA		4.0	4.5	5.0	V

AC CHARACTERISTICS

T_A = 25℃(unless otherwise noted)

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Uuit
K_{SVR} Power Supply ripple rejection	200 mV_{PP} ripple from 20 Hz–1 kHz, Gain = 20 dB, Inputs ac-coupled to AGND		70		dB
P_O Output power	THD+N=10%,f=1kHz,VCC=14V		24		W
THD+N Total harmonic distortion + noise	V_{CC} = 14 V, f = 1 kHz, Po = 12 W (half-power)		0.1		%
V_n Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		uV
			-80		dBV
Crosstalk	Vo=1Vrms,Gain=20dB,f=1kHz		-100		dB
SNR Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC} Oscillator frequency			315		kHz
Thermal trip point			170		℃
Thermal hysteresis			15		℃
Po Power Output	PO at 10% THD+N, VDD = 7.4V@RL = 2 Ω		12.5		W
	PO at 1% THD+N, VDD = 7.0V@RL = 2 Ω		10.0		
	PO at 10% THD+N, VDD = 9V@RL = 2 Ω		18.35		
	PO at 1% THD+N, VDD = 9V@RL = 2 Ω		15		
	PO at 10% THD+N, VDD = 12V@RL = 3 Ω		23.0		
	PO at 1% THD+N, VDD = 12V@RL = 3 Ω		19.0		
	PO at 10% THD+N, VDD = 12.0V@RL = 4 Ω		19.6		
	PO at 1% THD+N, VDD = 12.0V@RL = 4 Ω		16.0		
	PO at 1% THD+N, VDD = 18V@RL = 4Ω		32.0		
	PO at 10% THD+N, VDD = 18V@RL = 4 Ω		40.0		

TYPICAL CHARACTERISTICS

(All Measurements taken at 1 kHz, unless otherwise)

TOTALHARMONICDISTORTION
vs
FREQUENCY

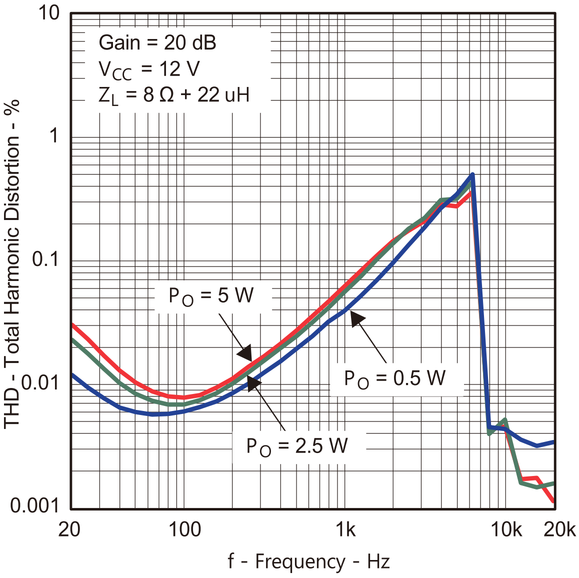


Figure2.

TOTALHARMONICDISTORTION
vs
FREQUENCY

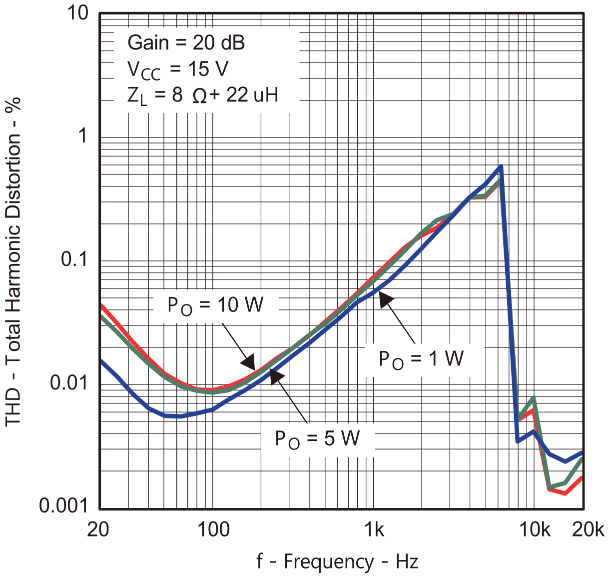


Figure3.

TOTALHARMONICDISTORTION
vs
FREQUENCY

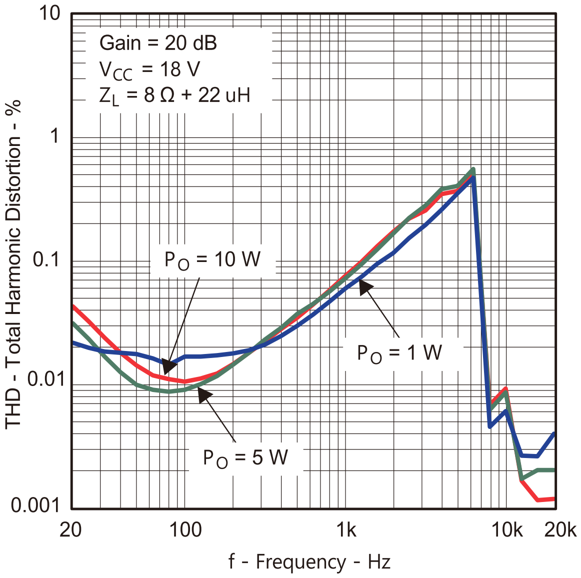


Figure4.

TOTALHARMONICDISTORTION
vs
FREQUENCY

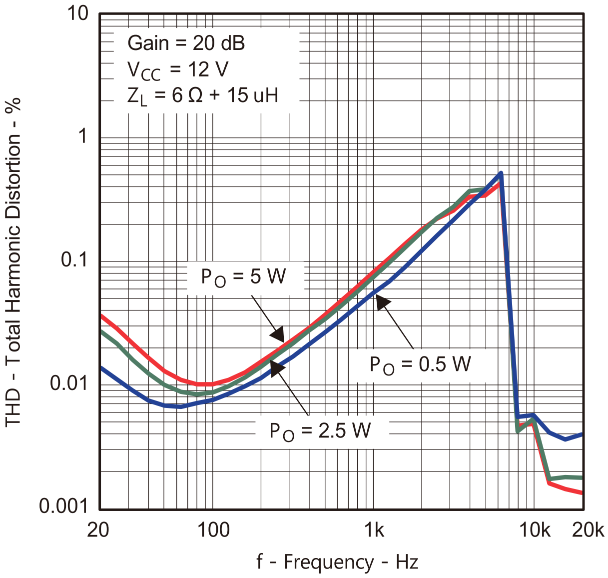


Figure5.

TOTALHARMONICDISTORTION
vs
FREQUENCY

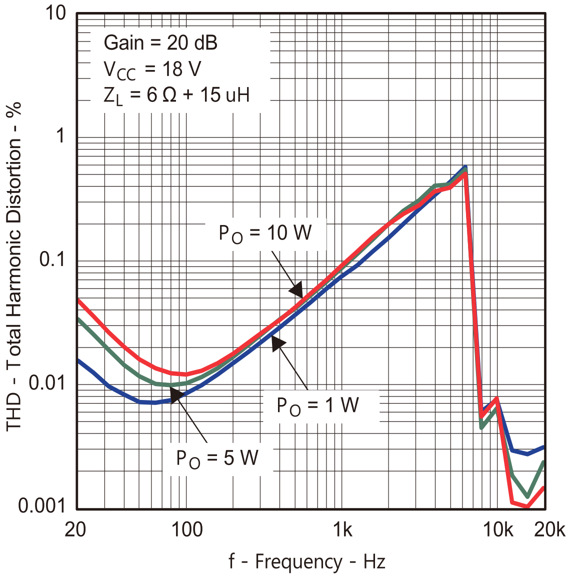


Figure6.

TOTALHARMONICDISTORTION
vs
FREQUENCY

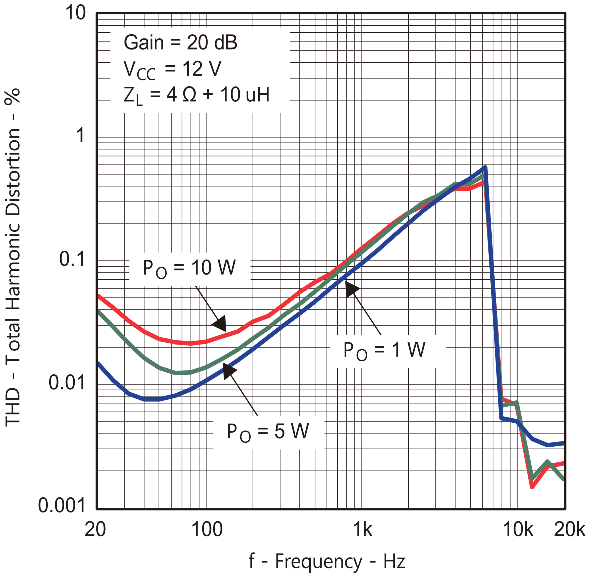


Figure7.

TOTALHARMONICDISTORTION+NOISE
vs
OUTPUTPOWER

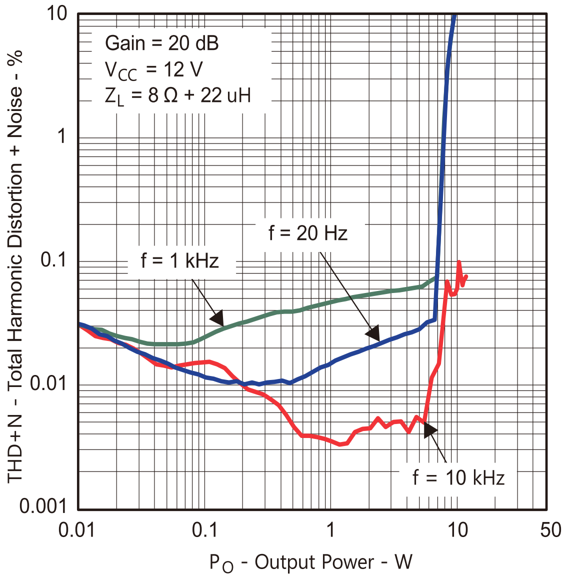


Figure8.

TOTALHARMONICDISTORTION+NOISE
vs
OUTPUTPOWER

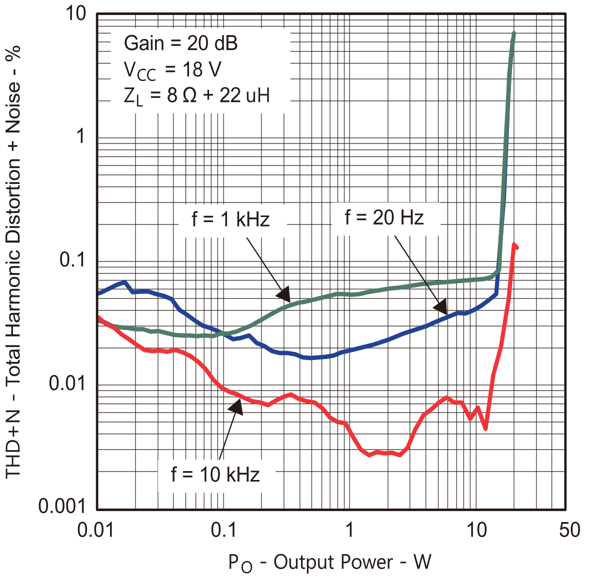


Figure9.

TOTALHARMONICDISTORTION+NOISE
vs
OUTPUTPOWER

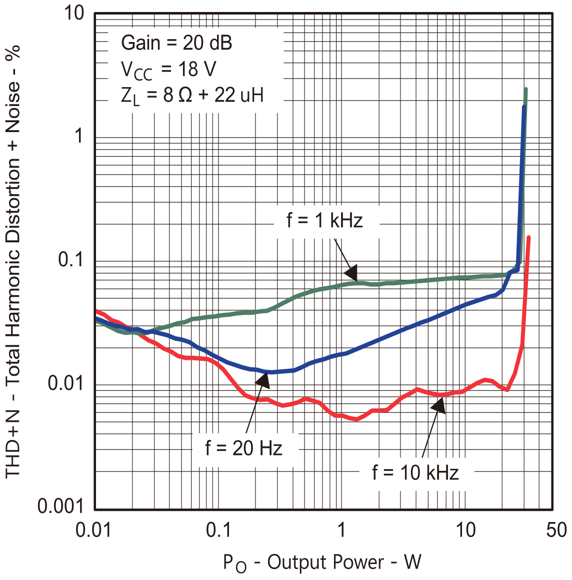


Figure10.

TOTALHARMONICDISTORTION+NOISE
vs
OUTPUTPOWER

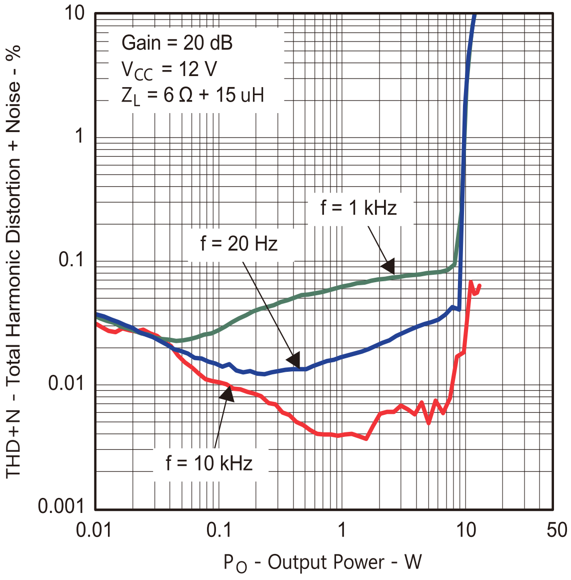


Figure11.

TOTALHARMONICDISTORTION+NOISE
vs
OUTPUTPOWER

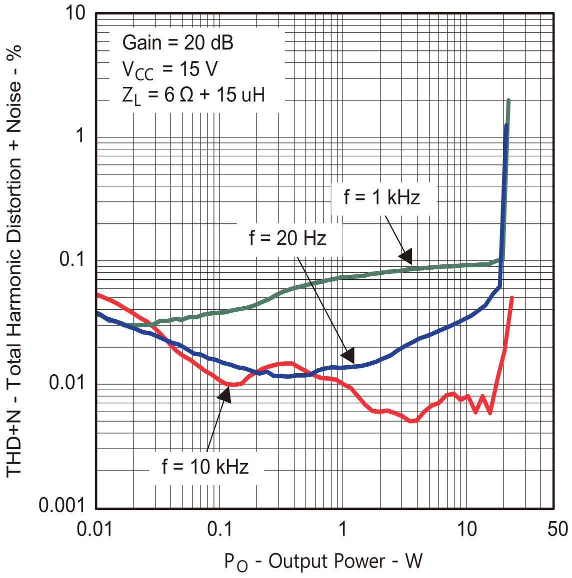


Figure12.

TOTALHARMONICDISTORTION+NOISE
vs
OUTPUTPOWER

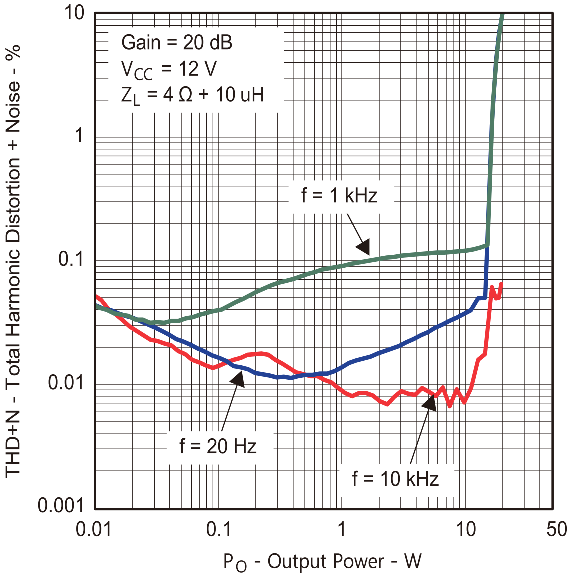
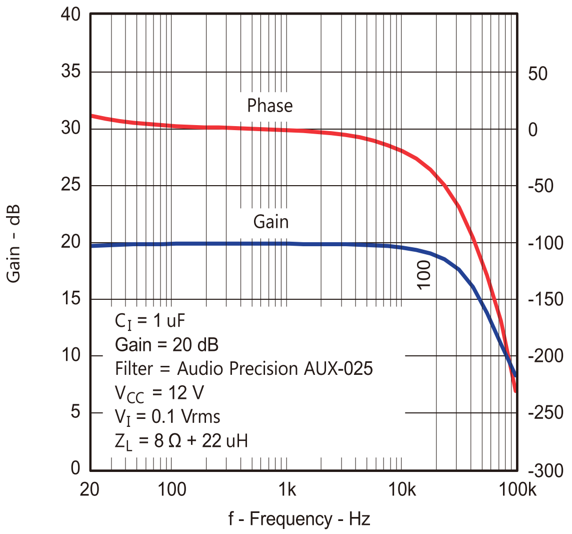
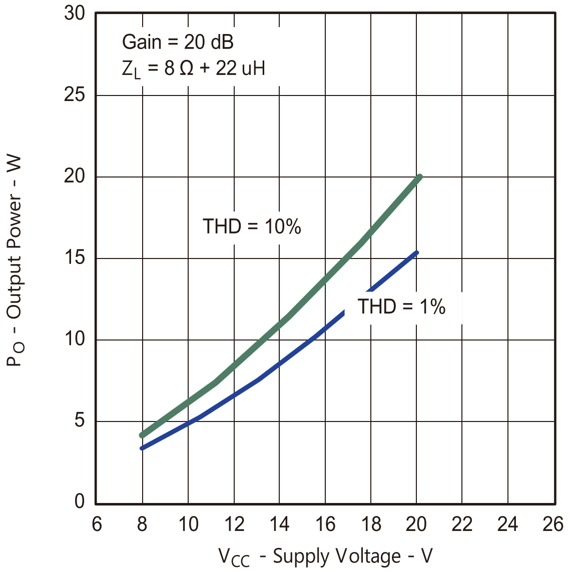


Figure13.



GAIN/PHASE
vs
FREQUENCY

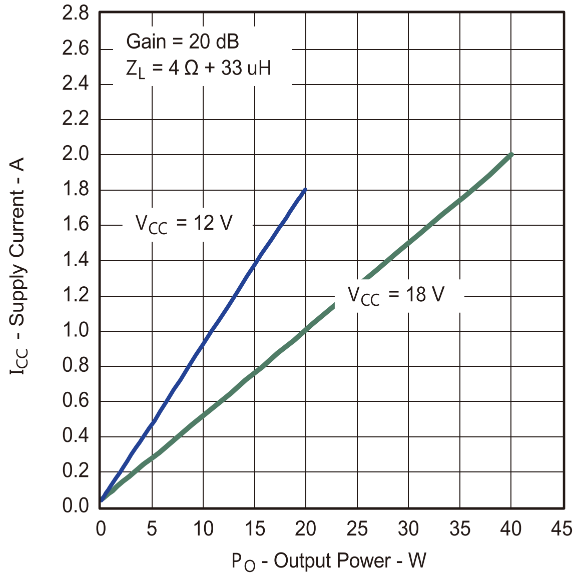
Figure14.



OUTPUTPOWER
vs
SUPPLYVOLTAGE

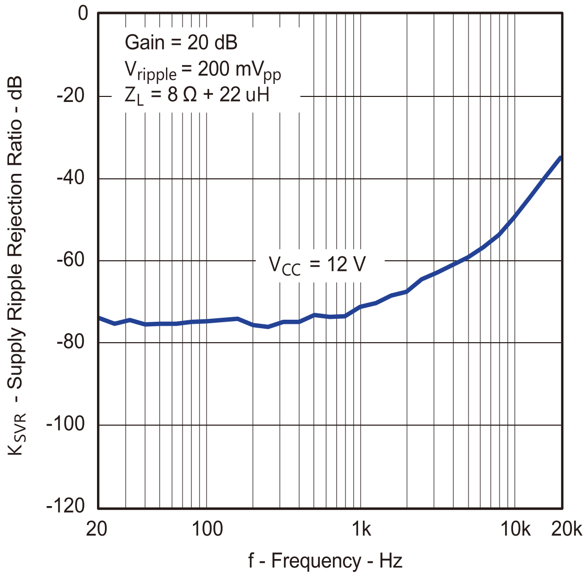
Note:DashedLinesrepresentthermallylimitedregions.

Figure15.



SUPPLYCURRENT
vs
OUTPUTPOWER

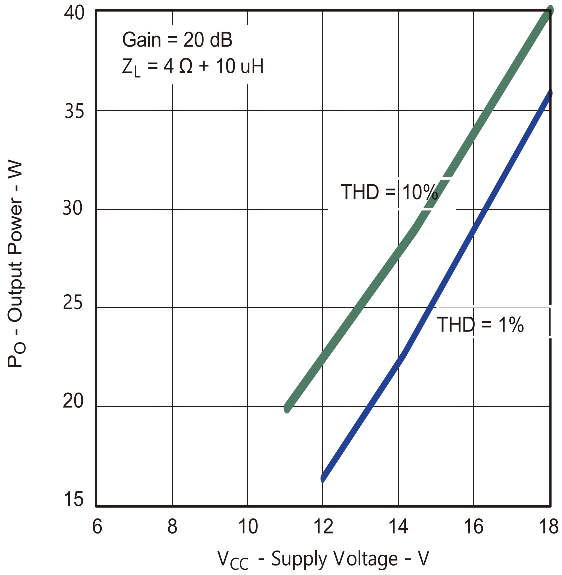
Figure16.



SUPPLYRIPPLEREJECTIONRATIO
vs
FREQUENCY

Figure17.

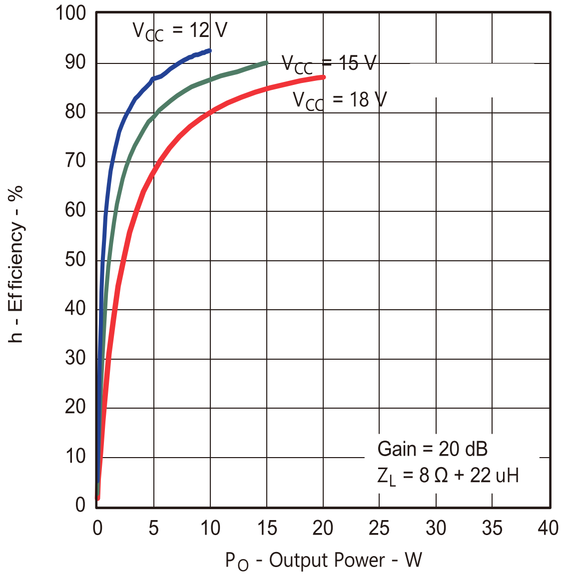
OUTPUTPOWER
vs
SUPPLYVOLTAGE



Note:DashedLinesrepresentthermallylimitedregions.

Figure18.

EFFICIENCY
vs
OUTPUTPOWER



Note:DashedLinesrepresentthermallylimitedregions.

Figure19.

EFFICIENCY
vs
OUTPUTPOWER(BTLwithLCFILTER)

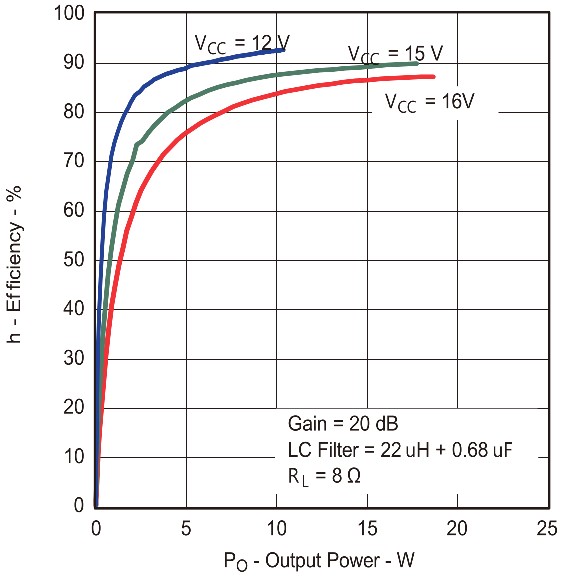
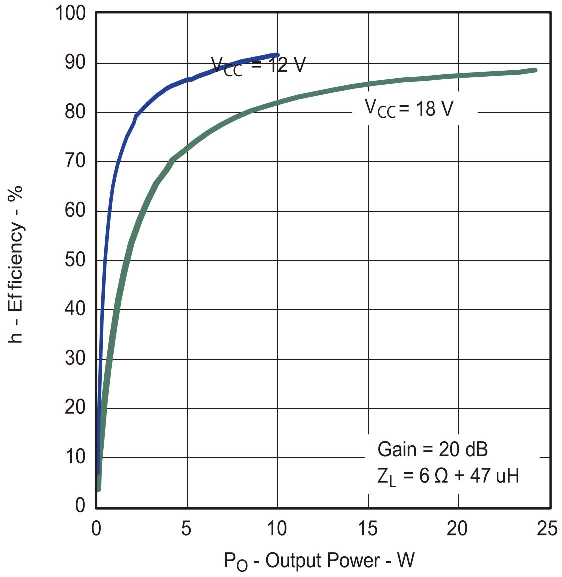


Figure20.

EFFICIENCY
vs
OUTPUTPOWER



Note:DashedLinesrepresentthermallylimitedregions.

Figure21.

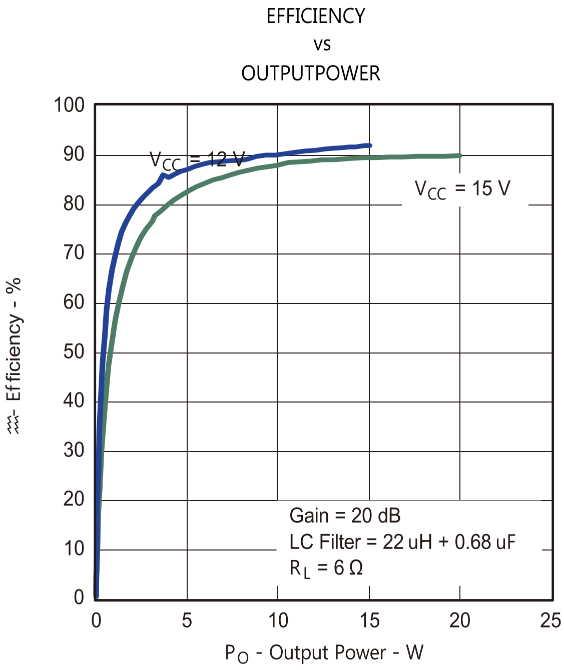


Figure22.

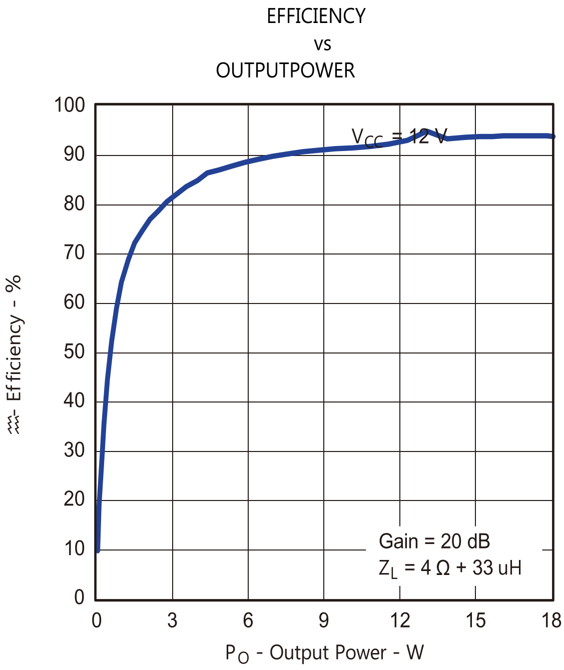


Figure23.

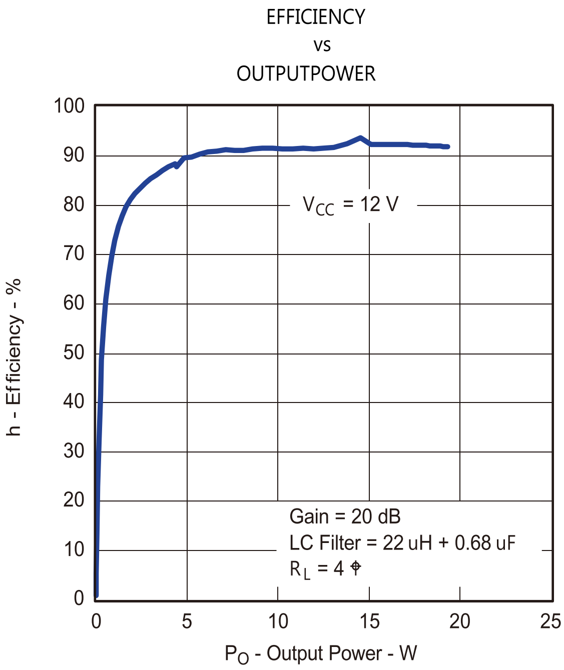
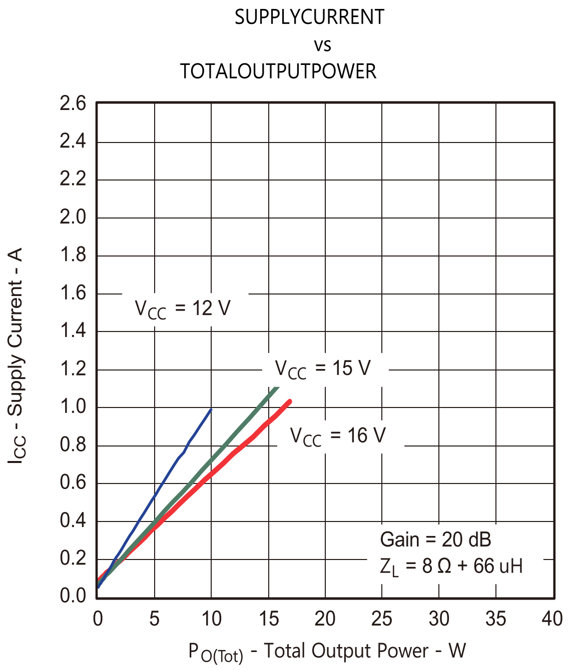


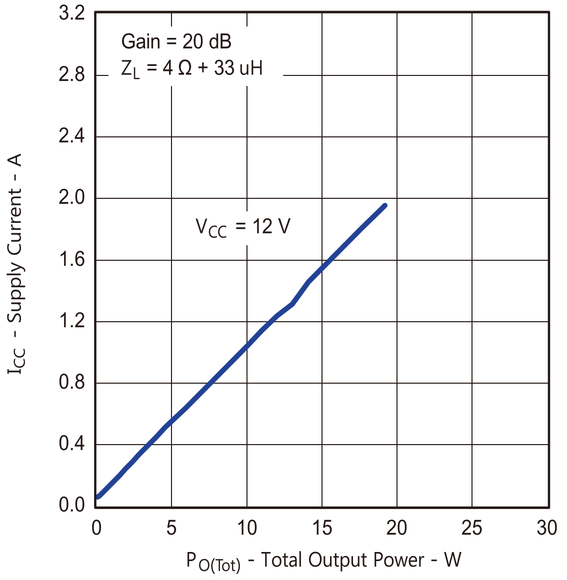
Figure24.



Note:DashedLinesrepresentthermallylimitedregions.

Figure25.

SUPPLYCURRENT
vs
TOTALOUTPUTPOWER



Note:DashedLinesrepresentthermallylimitedregions.

Figure26.

SUPPLYRIPPLEREJECTIONRATIO
vs
FREQUENCY

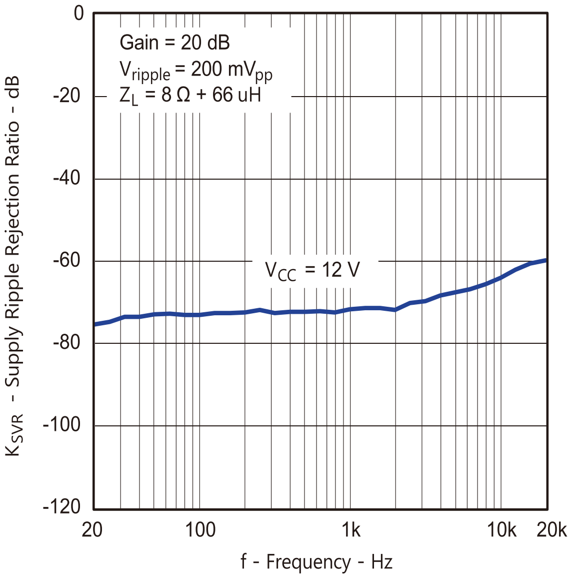


Figure27.

TOTALHARMONICDISTORTION
vs
FREQUENCY

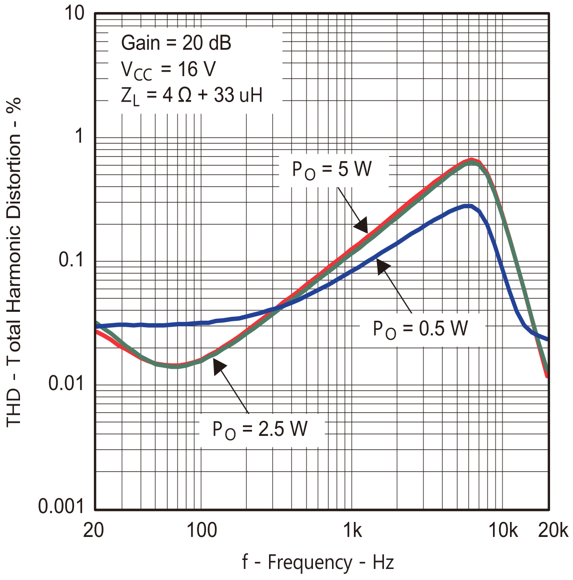


Figure28

Application Information

Gain Settings

CS8631E is fixed with 40 times gain, and the feedback resistance is internally integrated with 640K, and the integrated input resistance is 16k.

CRTL OPERATIONThe

CRTL input port should be at high potential when the op amp is working normally. When the CRTL is pulling at low potential, the output is turned off and the circuit enters standby mode.When the CRTL is between 1.15v and 1.25v,CS8631E enters spread spectrum mode. When the CTRL voltage is greater than 1.6v, the spread spectrum mode of CS8631E is turned off. Do not leave the CRTL unconnected because this will make the operational amplifier appear unpredictable.For optimal turn-off performance, place the operation in standby mode before turning off the power.The CRTL terminal is up to PVCC.

GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. Add a 1μF capacitor to ground at this pin.

THERMAL PROTECTION

Thermal protection on the CS8631E prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15° C. The device begins normal operation at this point with no external system interaction.

Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the CS8631E amplifier it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. it is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferritematerial is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the Class D amplifier. Many of the specifications regulating consumer less than 10 MHZ. electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30 MHZ and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should beAlso, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at very low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class D outputs to ground. Suggested values for a simple RC series snubber network would be 10 ohms in series with a 330 pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the PGND or the PowerPad™ beneath the chip.

Efficiency: LC Filter Required With the Traditional Class-D Modulation Scheme

The main reason that the traditional classD amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 x Vcc, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The CS8631E modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is Vcc instead of 2 x Vcc. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed. An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flowthrough the filter instead of the load. The filter has less resistance but higher impedance at the switchingfrequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

When to Use an Output Filter for EMI Suppression

The CS8631E has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 125 cm and high power. The CS8631E EVM passes FCC Class B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency. There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are circuits near which are sensitive to noise. Therefore, a classic second order Butterworth filter similar to those shown in Figure A through Figure B can be used.

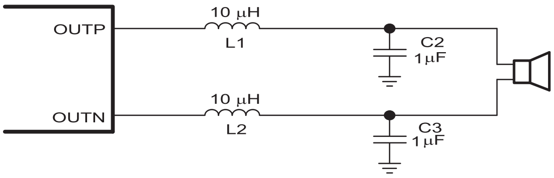


Figure A. Typical LCOutput Filter, Cutoff Frequency of 27kHz,Speaker Impedance =4Ω

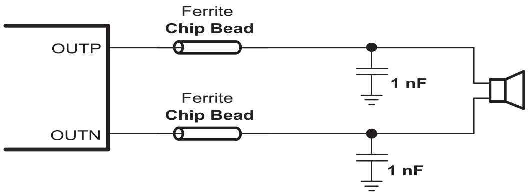
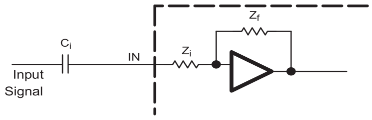


Figure B. Typical Ferrite Chip Bead Filter (Chip Bead Example:)

Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, kΩ ±20%, to the largest value, 60 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.



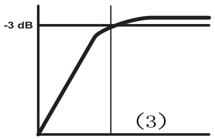
The -3-dB frequency can be calculated using Equation 2. Use the ZI values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i}$$

Input Capacitor, CI

In the typical application, an input capacitor (CI) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, CI and the input impedance of the amplifier (ZI) form a highpass filter with the corner frequency determined in Equation 3.

$$f_c = \frac{1}{2\pi Z_i C_i} \tag{3}$$



The value of CI is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where ZI is 60 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 3 is reconfigured as Equation 4.

$$C_i = \frac{1}{2\pi Z_i f_c} \tag{4}$$

In this example, CI is 0.13 μF; so, one would likely choose a value of 0.15 μF as this value is commonly used. If the gain is known and is constant, use ZI from Table 1 to calculate CI. A further consideration for this capacitor is the leakage path from the input source through the input network (CI) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 3 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned

Power Supply Decoupling, CS

The CS8631E is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond wire and copper trace inductances as well as lead frame capacitance, a good quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor should be placed as close to the device PVCC pins and system ground (either PGND pins or PowerPad) as possible. For mid-frequency noise due to filter resonances or PWM switching transients as well as digital hash on the line, another good quality capacitor typically 0.1 μF to 1 μF placed as close as possible to the device PVCC leads works best For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 μF or greater placed near the audio power amplifier is recommended. The 220 μF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs.

The PVCC terminals provide the power to the output transistors, so a 220 μF or larger capacitor should be placed on each PVCC terminal. A 10 μF capacitor on the AVCC terminal is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency class D noise from entering the linear input amplifiers.

BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22 μF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22 μF capacitor must be connected from OUTPx to BSPx, and one 0.22 μF capacitor must be connected from OUTNx to BSNx. (See the application circuit diagram in Figure 1.)

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

Differential Inputs

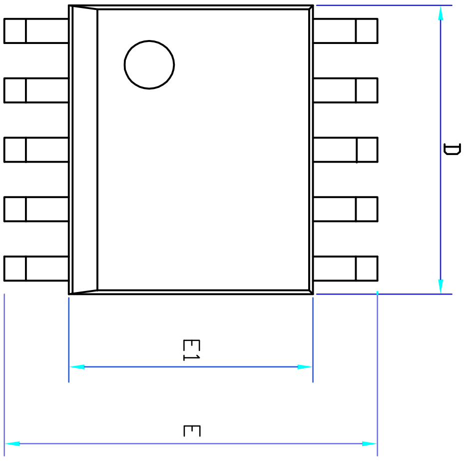
The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the CS8631E with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the CS8631E with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

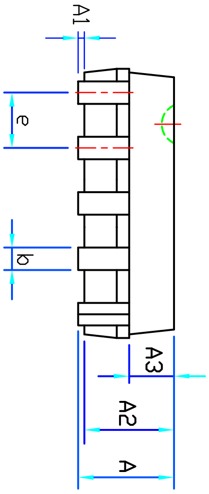
The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 14 ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

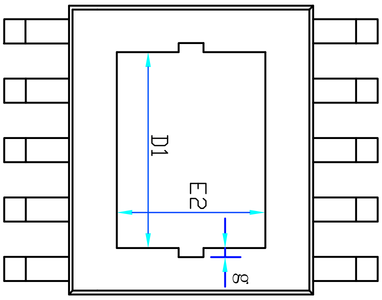
Using Low-ESR Capacitors

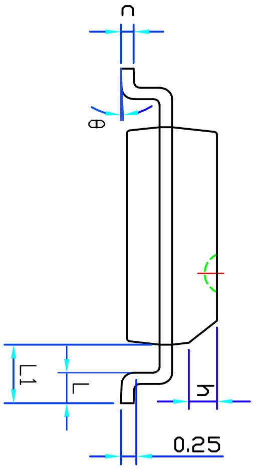
Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

Package Information CS8631E ESOP10L









SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	—	—	1.50
A1	0.02	0.05	0.08
A2	1.30	1.40	1.50
A3	0.70	0.75	0.80
b	0.35	—	0.45
c	0.20	—	0.24
D	4.80	4.90	5.00
D1	3.10REF		
e	1.00BSC		
E	6.05	6.15	6.25
E1	3.82	3.92	4.02
E2	2.20REF		
L	0.50	—	0.70
L1	1.15REF		
h	0.30	0.40	0.50
θ	0	—	8°
g	0.15REF		