50W Filter-Free MONO ClassD Audio Power Amplifier

FEATURES

- PO= 19W RL=4Ω @THD+N=10% VDD=12.5V
- PO= 47W RL=4Ω @THD+N=10% VDD=19V
- PO= 50W RL=6Ω @THD+N=10% VDD=23V
- 90% Efficient ClassD Operation into 8Ω Load Eliminates Need for Heat Sinks
- Supply Voltage Range: Operation from5.5 to 23V
- Filter-Free Operation
- Flow Through Pin Out Facilitates Easy Board Layout
- Robust Pin-to-Pin Short Circuit Protection and Thermal Protection with Auto-Recovery Option
- Excellent THD+N/ Pop Free Performance
- Four Selectable, Fixed Gain Settings
- Differential Inputs

APPLICATIONS

- Televisions
- Consumer Audio Equipment

DESCRIPTION

The CS8626E is a 50W efficient, ClassD audio power amplifier for driving a bridge tied speaker.Advanced EMI Suppression Technology enables the use of inexpensive ferrite bead filters at the outputs while meeting EMC requirements. SpeakerGuard™ speaker protection system includes an adjustable power limiter. The adjustable power limiter allows the user to set a "virtual" voltage rail lower than the chip supply to limit the amount of current through the speaker.

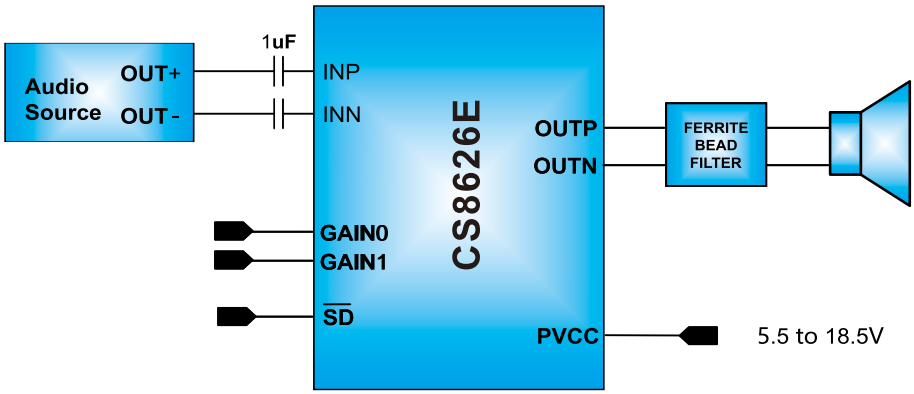
The CS8626E can drive a mono speaker as low as 4Ω. The high efficiency of the CS8626E > 90%,eliminates the need for an external heat sink when playing music.

The outputs are fully protected against shorts to GND, VCC, and output-to-output. The short-circuit protection and thermal protection includes an auto-recovery feature.

Package

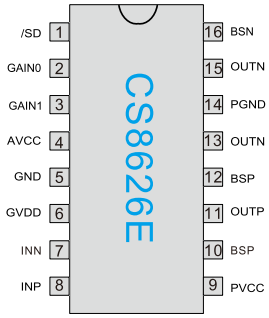
ESOP16

Typical Application



Differential Input Configuration

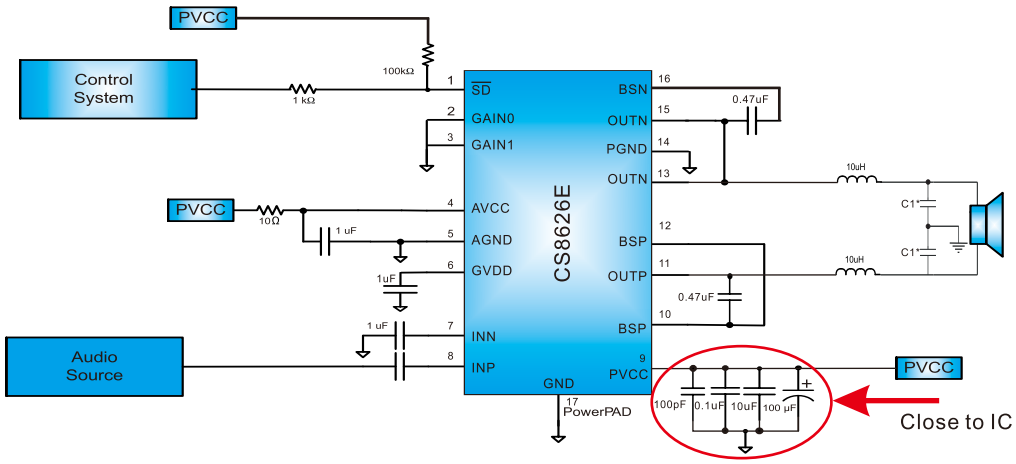
Pin Descriptions



ESOP16L
(Top View)

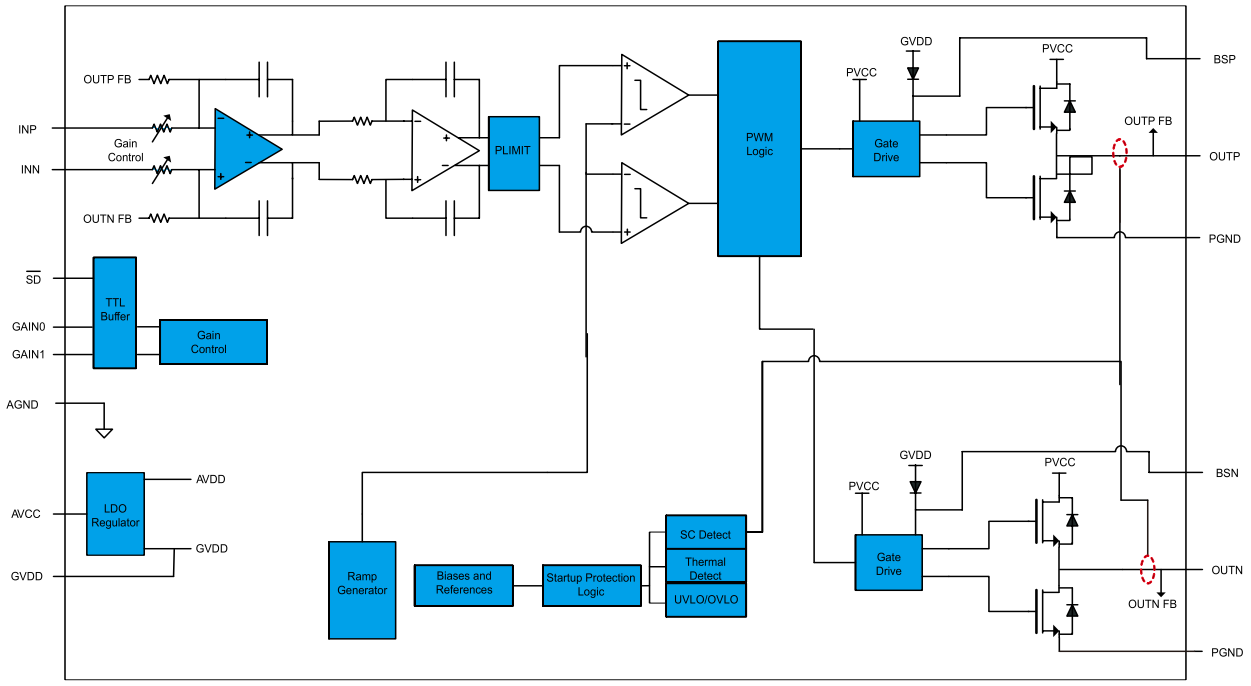
NUMBER	NAME	I/O/P	DESCRIPTION
1	/SD	I	Shutdown logic input for audio amp (LOW =outputs Hi-Z, HIGH =outputs enabled). TTL logic levels with compliance to AVCC.
2	GAIN0	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
3	GAIN1	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.
4	AVCC	P	Analog supply
5	AGND	P	Analog signal ground. Connect to the thermal pad.
6	GVDD	P	High-side FET gate drive supply.
7	INN	I	Negative audio input, Biased at 3V.
8	INP	I	Positive audio input, Biased at 3V.
9	PVCC	P	Power supply
10	BSP	I	Bootstrap I/O, positive high-side FET.
11	OUTP	O	Class-D H-bridge positive output
12	BSP	I	Bootstrap I/O, positive high-side FET.
13	OUTN	O	Class-D H-bridge negative output.
14	PGND	P	Power ground for the H-bridges.
15	OUTN	O	Class-D H-bridge negative output.
16	BSN	I	Bootstrap I/O , negative high-side FET.

Typical Application



Single-ended Input Configuration

Block Diagram



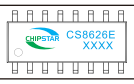
over operating free-air temperature range(unless otherwise noted)(1)

			单位
V_{CC}	Supply voltage	AVCC,PVCC	0.3Vto23V
V_I	Interface pin voltage	SD,GAIN0,GAIN1	0.3VtoV_{CC}+0.3V
		INN,INP	0.3Vto6.3V
T_A	Operating free-air temperature range		-40℃ to 85℃
T_J	Operating junction temperature range		-40℃to150℃
T_{stg}	Storage temperature range		-65℃ to150℃
R_L	Load	BTL:PVCC>15V	4.8
		BTL:PVCC ≤15V	3.2

Thermal information[2]

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	45	℃/W
θ_{JC}	Junction-to-case (top) thermal resistance	10	℃/W
θ_{JB}	Junction-to-board thermal resistance	17.5	℃/W

Order Information

Device	Package	Making	Reel Size	Tape Width	Quantity
CS8626E	ESOP16L		Tube		50

ESD Range

ESD HBM mode ---------- ±2kV
ESD MM mode ----------±400V

1,The ThermalPad on the bottom of the IC should soldered directly to the PCB's ThermalPad area that with several thermal vias connect to the ground plan,and the PCB is a 2-layer,5-inch square area with 2oz copper thickness.
2,Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device.Functional operation at conditions other than the operating conditions specified is not implied.Only one Absolute Maximum Rating should be applied at one time.

Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	Min	Max	Unit
V_{CC}	Supply voltage	PVCC,AVCC	5.5	23	V
V_{IH}	"H" input voltage	$\overline{SD}$,GAIN0,GAIN1	2		V
V_{IL}	"L" input voltage	$\overline{SD}$,GAIN0,GAIN1		0.8	V
V_{OL}	"H" output voltage	$R_{PULL-UP}$ =100k,V_{CC} =15V		0.8	V
I_{IH}	"H" input current	$\overline{SD}$,GAIN0,GAIN1,V_I =2V,V_{CC}=15V		50	uA
I_{IL}	"L" input current	$\overline{SD}$,GAIN0,GAIN1,V_I=0.8V,V_{CC}=15V		5	uA

DC CHARACTERISTICS T_A = 25 C, V_{CC} = 12 V, RL = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		Min	Typ	Max	Uuit
$\|V_{OS}\|$	Offset Voltage	V_I =0V,Gain=36dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$=2V,no load,PV_{CC}=24V			15	20	mA
$I_{CC(SD)}$	Quiescent supply current in sd mode	$\overline{SD}$=0.8V,no load,PV_{CC}=24V			60	150	uA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} =12V,I_O=500mA, T_J =25℃	High Side		200		mΩ
			Low side		200		
G	Gain	GAIN1=0.8V	GAIN0=0.8V	19	20	21	dB
			GAIN0=2V	25	26	27	
		GAIN1=2V	GAIN0=0.8V	31	32	33	dB
			GAIN0=2V	35	36	37	
t_{on}	Turn-on time	$\overline{SD}$=2V			110		ms
t_{OFF}	Turn-off time	$\overline{SD}$=0.8V			2		us
GVDD	Gate Drive Supply	I_{GVDD} =100 mA		4.0	4.5	5.0	V

DC CHARACTERISTICS T_A = 25 C, V_{CC} = 12 V, RL = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		Min	Typ	Max	Uuit
$\|V_{OS}\|$	Offset Voltage	V_I =0V,Gain=36dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$=2V,no load,PV_{CC} =12V			20	25	mA
$I_{CC(SD)}$	Quiescent supply current in sd mode	$\overline{SD}$=0.8V,no load,PV_{CC} =12V			200		uA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} =12V,I_O=500mA, T_J =25℃	High Side		200		mΩ
			Low side		200		
G	Gain	GAIN1=0.8V	GAIN0=0.8V	19	20	21	dB
			GAIN0=2V	25	26	27	
		GAIN1=2V	GAIN0=0.8V	31	32	33	dB
			GAIN0=2V	35	36	37	
t_{on}	Turn-on time	$\overline{SD}$=2V			110		ms
t_{OFF}	Turn-off time	$\overline{SD}$=0.8V			2		us
GVDD	Gate Drive Supply	I_{GVDD} =2mA		4.0	4.5	5.0	V

AC CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, RL = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	Min	Typ	Max	Uuit
K_{SVR}	Power Supply ripple rejection	200 mV_{PP} ripple from 20 Hz–1 kHz, Gain = 20 dB, Inputs ac-coupled to AGND		70		dB
P_O	Output power	THD+N=10%,f=1kHz,VCC=19V,RL=4Ω		47		W
THD+N	Total harmonic distortion + noise	V_{CC} = 14 V, f = 1 kHz, P_O = 12 W (half-power)		0.1		%
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		uV
				-80		dBV
	Crosstalk	Vo=1Vrms,Gain=20dB,f=1kHz		-100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			170		℃
	Thermal hysteresis			15		℃

AC CHARACTERISTICS

T_A = 25 C, V_{CC} = 12V, RL = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	Min	Typ	Max	Uuit
K_{SVR}	Power Supply ripple rejection	200 mV_{PP} ripple from 20 Hz–1 kHz, Gain = 20 dB, Inputs ac-coupled to AGND		-70		dB
P_O	Output power	THD+N=10%,f=1kHz,VCC=23V,RL=4Ω		50		W
THD+N	Total harmonic distortion + noise	V_{CC} = 12.5 V, f = 1 kHz, P_O = 9W (half-power)		0.06		%
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		65		uV
				-80		dBV
	Crosstalk	Vo=1Vrms,Gain=20dB,f=1kHz		-100		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency		250	310	350	kHz
	Thermal trip point			170		℃
	Thermal hysteresis			20		℃

TYPICAL CHARACTERISTICS

(All Measurements taken at 1 kHz, unless otherwise)

TOTALHARMONICDISTORTION
vs
FREQUENCY(BTL)

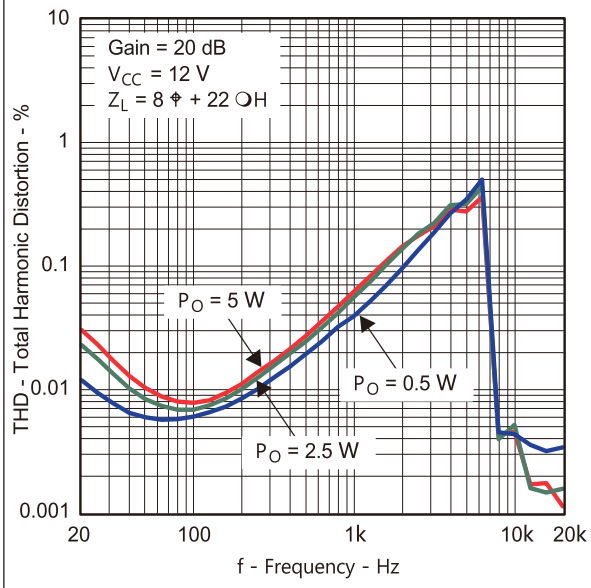


Figure2.

TOTALHARMONICDISTORTION
vs
FREQUENCY(BTL)

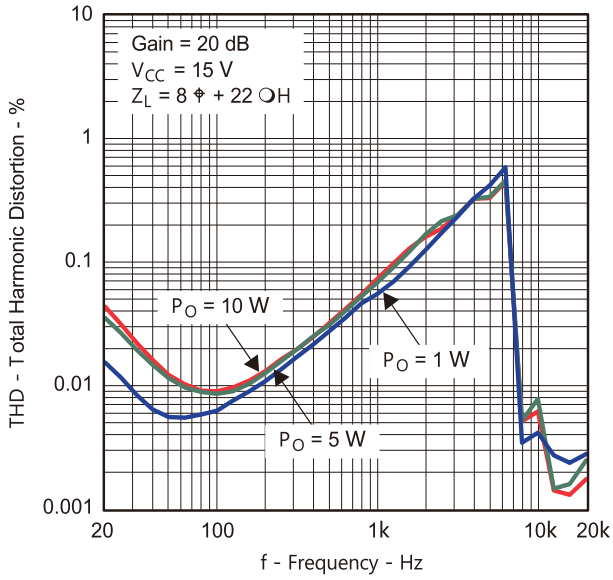


Figure3.

TOTALHARMONICDISTORTION
vs
FREQUENCY(BTL)

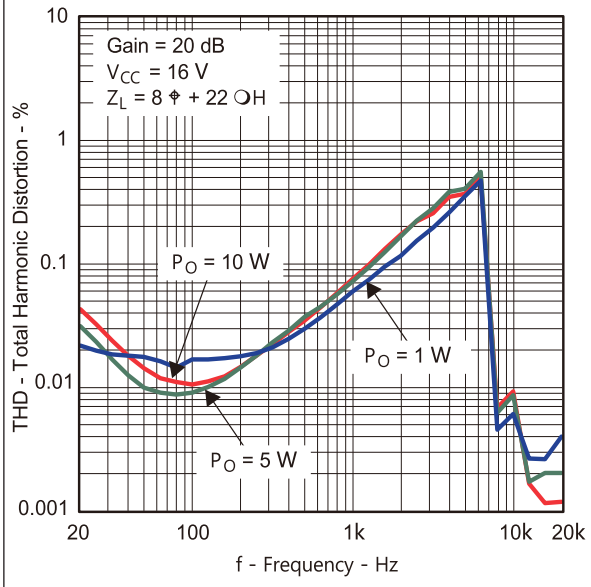


Figure4.

TOTALHARMONICDISTORTION
vs
FREQUENCY(BTL)

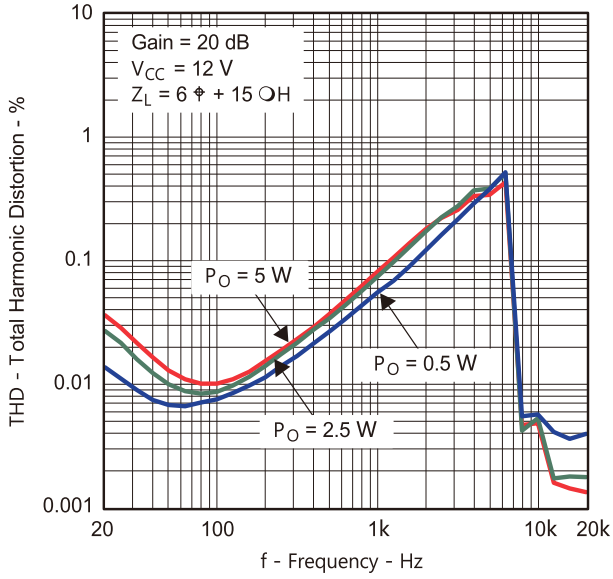


Figure5.

TOTALHARMONICDISTORTION
vs
FREQUENCY(BTL)

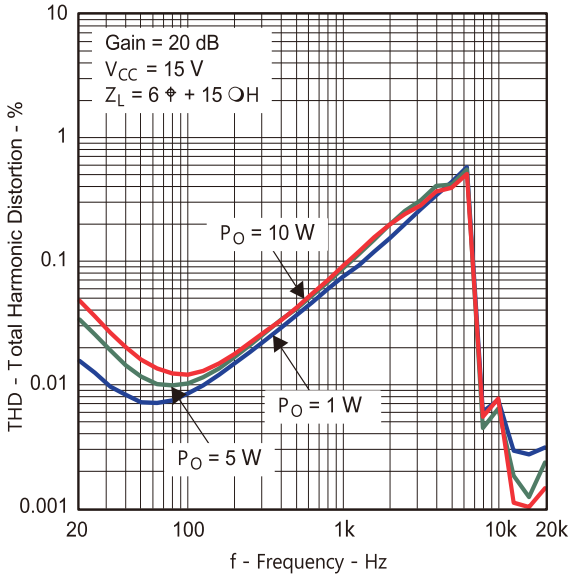


Figure6.

TOTALHARMONICDISTORTION
vs
FREQUENCY(BTL)

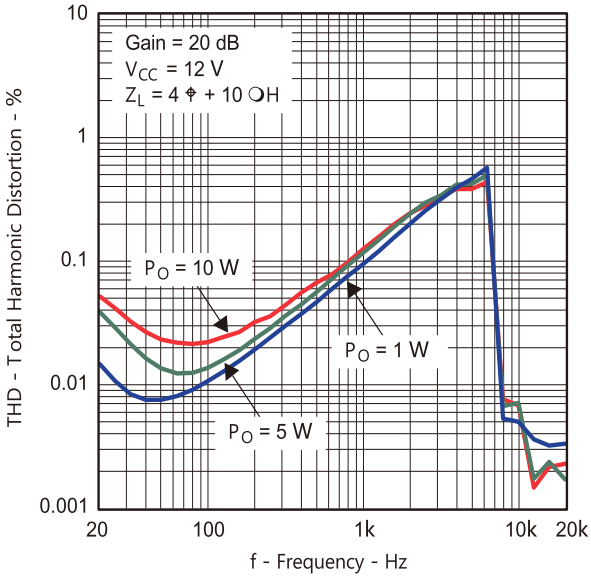


Figure7.

TOTALHARMONICDISTORTION+NOISE
vs
OUTPUTPOWER(BTL)

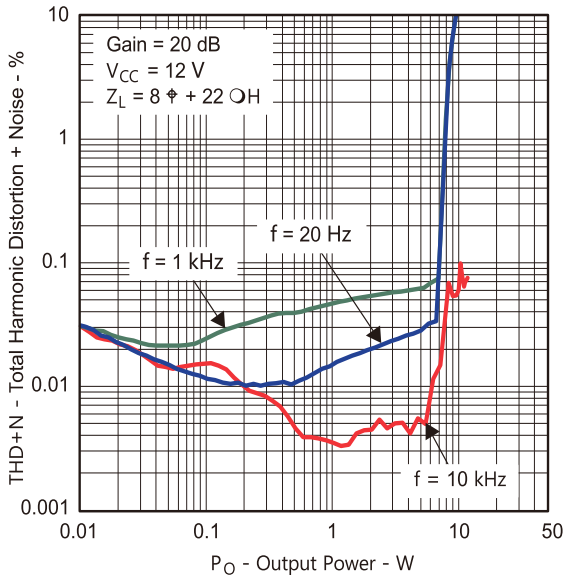


Figure8.

TOTALHARMONICDISTORTION+NOISE
vs
OUTPUTPOWER(BTL)

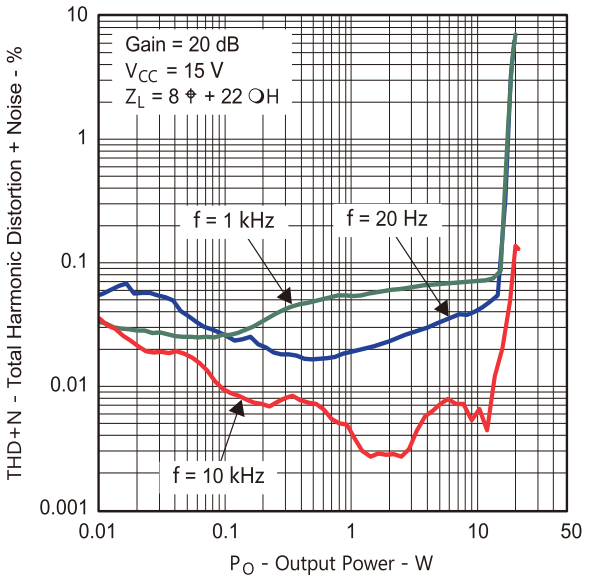


Figure9.

TOTALHARMONICDISTORTION+NOISE
vs
OUTPUTPOWER(BTL)

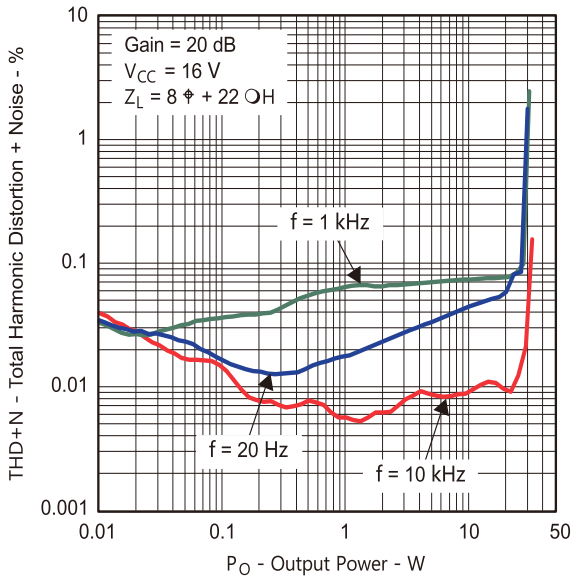


Figure10.

TOTALHARMONICDISTORTION+NOISE
vs
OUTPUTPOWER(BTL)

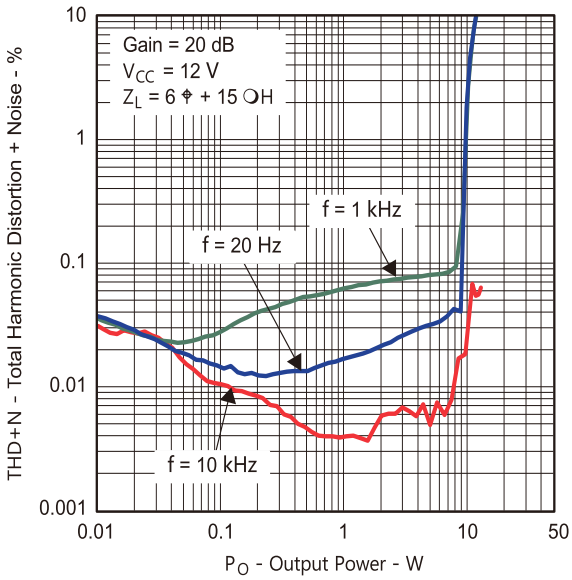


Figure11.

TOTALHARMONICDISTORTION+NOISE
vs
OUTPUTPOWER(BTL)

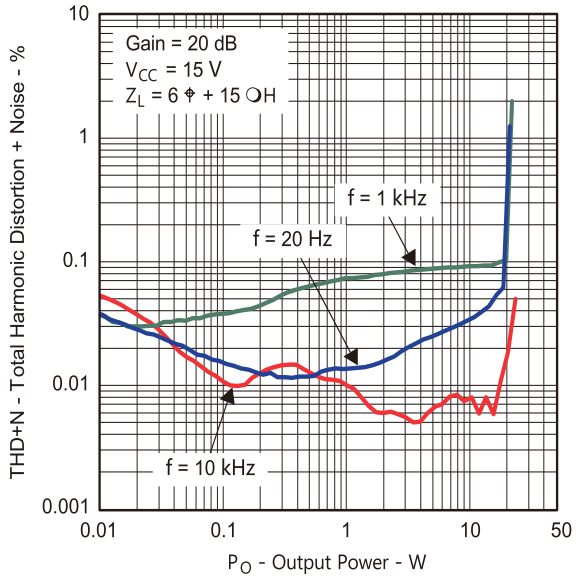


Figure12.

TOTALHARMONICDISTORTION+NOISE
vs
OUTPUTPOWER(BTL)

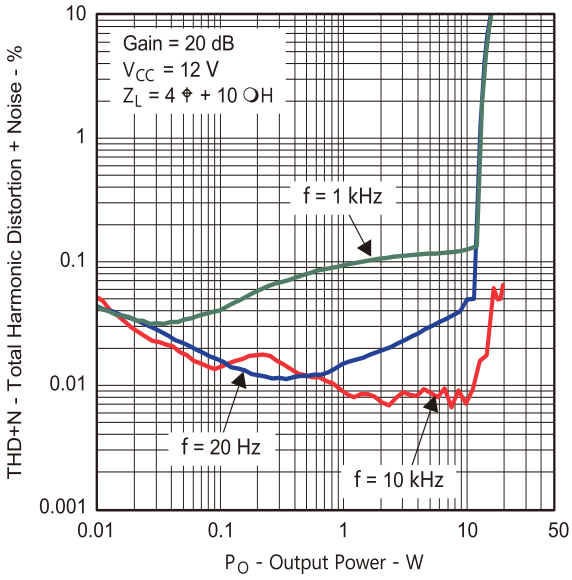


Figure13.

Application Information

Gain setting via GAIN0 and GAIN1 inputs

The gain of the CS8626E is set by two input terminals, GAIN0 and GAIN1. The voltage slew rate of these gain terminals, along with terminals 1 and 14, must be restricted to no more than 10V/ms.For higher slew rates, use a 100kΩ resistor in series with the terminals.

The gains listed in Table 1 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (ZI) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by +/-20% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 7.2 kΩ, which is the absolute minimum input impedance of the CS8626E. At the lower gain settings, the input impedance could increase as high as 72 kΩ

Table 1.Gain Setting

GAIN1	GAIN0	GAIN	Rin (kΩ)	Rf (kΩ)
0	0	10	20	200
0	1	22	13	290
1	0	43	7.87	340
1	1	70	5.25	368

The CS8626E employs a shutdown mode of operation designed to reduce supply current (ICC) to the absolute minimum level during periods of nonuse for power conservation. The SD input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SD low causes the outputs to mute and the amplifier to enter a low-current state. Never leave SD unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage

$\overline{SD}$ OPERATION

The CS8626E employs a shutdown mode of operation designed to reduce supply current (Icc) to the absolute minimum level during periods of nonuse for power conservation. The SD input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SD low causes the outputs to mute and the amplifier to enter a low-current state. Never leave SD unconnected, because amplifier

operation would be unpredictable. For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. Add a 1μF capacitor to ground at this pin.

THERMAL PROTECTION

Thermal protection on the CS8626E prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15° C. The device begins normal operation at this point with no external system interaction.

Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the CS8626E amplifier it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. it is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferritematerial is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the Class D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30 MHZ and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead current handling capability by measuring the resonant frequency of the filter output at very low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class D outputs to ground. Suggested values for a simple RC series snubber network would be 10 ohms in series with a 330 pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the PGND or the PowerPad™ beneath the chip.

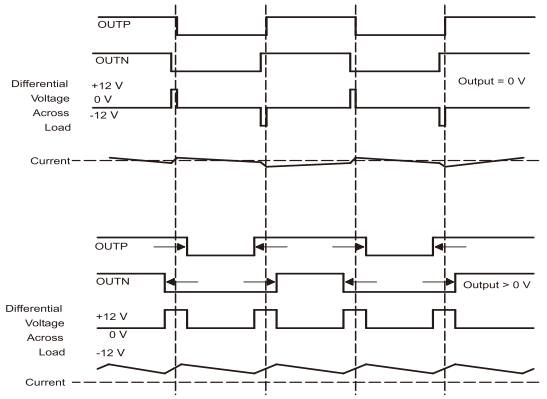
Efficiency: LC Filter Required With the Traditional Class-D Modulation Scheme

The main reason that the traditional classD amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 x Vcc, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive. The CS8626E modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is Vcc instead of 2 x Vcc. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed. An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flowthrough the filter instead of the load. The filter has less resistance but higher impedance at the switchingfrequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

Modulation Scheme

The CS8626E uses a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load. Each output is switching from 0 volts to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of

OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any I2R losses in the load.



TheT CS8626E OutputVoltageandCurrentWaveformsIntoanInductiveLoad

When to Use an Output Filter for EMI Suppression

The CS8626E has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 125 cm and high power. The CS8626E EVM passes FCC Class B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency. There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are circuits near which are sensitive to noise. Therefore, a classic second order Butterworth filter similar to those shown in Figure A through Figure C can be used.

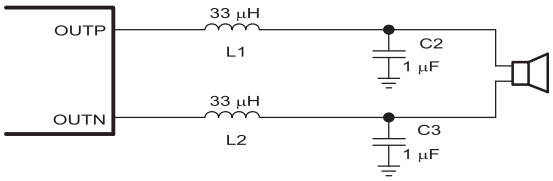


Figure A. Typical LCOutput Filter, Cutoff Frequency of 27kHz,Speaker Impedance =8Ω

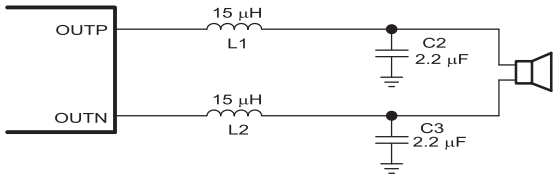


Figure B. Typical LCOutput Filter, Cutoff Frequency of 27kHz,Speaker Impedance =4Ω

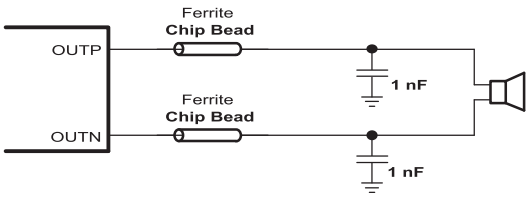
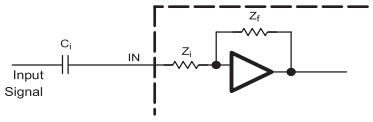


Figure C. Typical Ferrite Chip Bead Filter (Chip Bead Example:)

Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 9 kΩ ±20%, to the largest value, 60 kΩ ±20%. As a result, if a single capacitor is used in the input high-pass filter, the -3 dB or cutoff frequency may change when changing gain steps.



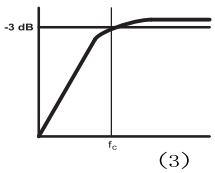
The -3-dB frequency can be calculated using Equation 2. Use the ZI values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i}$$

Input Capacitor, CI

In the typical application, an input capacitor (CI) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, CI and the input impedance of the amplifier (ZI) form a highpass filter with the corner frequency determined in Equation 3.

$$f_c = \frac{1}{2\pi Z_i C_i} \qquad (3)$$



The value of CI is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where ZI is 60 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 3 is reconfigured as Equation 4.

$$C_i = \frac{1}{2\pi Z_i f_c} \qquad (4)$$

In this example, CI is 0.13 µF; so, one would likely choose a value of 0.15 µF as this value is commonly used. If the gain is known and is constant, use ZI from Table 1 to calculate CI. A further consideration for this capacitor is the leakage path from the input source through the input network (CI) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 3 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

Power Supply Decoupling, CS

The CS8626E is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond wire and copper trace inductances as well as lead frame capacitance, a good quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor should be placed as close to the device PVCC pins and system ground (either PGND pins or PowerPad) as possible. For mid-frequency noise due to filter resonances or PWM switching transients as well as digital hash on the line, another good quality capacitor typically 0.1 µF to 1 µF placed as close as possible to the device PVCC leads works best For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 µF or greater placed near the audio power amplifier is recommended. The 220 µF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs.

The PVCC terminals provide the power to the output transistors, so a 220 µF or larger capacitor should be placed on each PVCC terminal. A 10 µF capacitor on the AVCC terminal is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency class D noise from entering the linear input amplifiers.

BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22 µF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22 µF capacitor must be connected from OUTPx to BSPx, and one 0.22 µF capacitor must be connected from OUTNx to BSNx. (See the application circuit diagram in Figure 1.)

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the CS8626E with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the CS8626E with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 14 ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

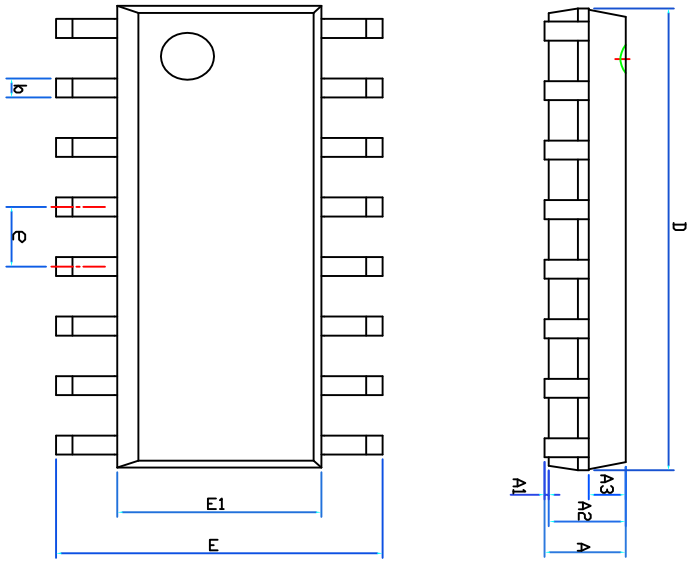
Printed-Circuit Board (PCB) Layout

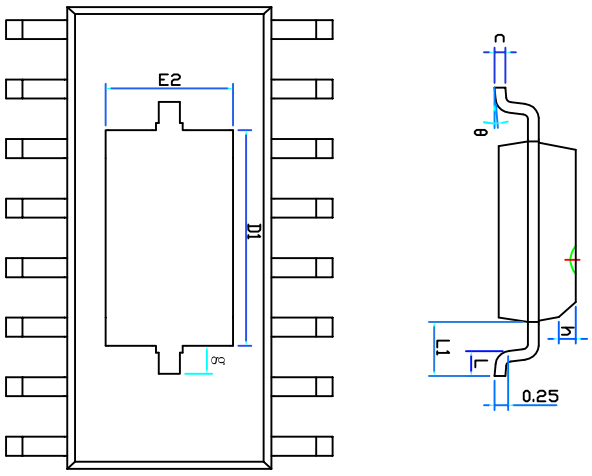
The CS8626E can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed help to meet EMC requirements.

- Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220 µF or greater) bulk power supply decoupling capacitors should be placed near the CS8626E on the PVCCL and PVCCR supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1000 pF and a larger mid-frequency cap of value between 0.1µF and 1µF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to PGND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding—The AVCC decoupling capacitor should be grounded to analog ground The PVCC decoupling capacitors should connect to PGND. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the CS8626E.
- Output filter—The ferrite EMI filter (Figure 43) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter (Figure 41 and Figure 42) should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground.
- Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be 6.46mm by 2.35mm. Seven rows of solid vias (three vias per row, 0,3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias.

Package Information

CS8626E ESOP16L





SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	—	—	1.55
A1	0.02	0.05	0.08
A2	1.40	1.45	1.50
A3	0.70	0.75	0.80
b	0.35	—	0.45
c	0.20	—	0.24
D	9.70	9.80	9.90
D1	4.60REF		
e	1.27BSC		
E	6.25	6.35	6.45
E1	3.70	3.80	3.90
E2	2.40REF		
L	0.50	—	0.70
L1	1.25REF		
h	0.25	0.35	0.45
θ	0	—	8°
g	0.60REF		