For Single Cell Lithium Battery Powered, Mute Function, Three Adaptive Boost Points Two Anti–Clipping Options, AB/D, 2X8W Class R Stereo Audio Power Amplifier

General Description

The CS83826C is a Class R stereo audio power amplifier designed for single-cell lithium battery-powered applications. It features fixed gain, two anti-clipping modes, AB/D mode switching, a mute function, and a built-in BOOST voltage boost module. When powered by a single-cell lithium battery, the CS83826C can drive speakers as low as 4Ω, delivering a maximum constant output power of 2X8W@10% THD (Total Harmonic Distortion). Equipped with three adaptive boost points, the CS83826C automatically selects the appropriate boost point based on the input audio signal level. This optimization maximizes the efficiency of the power amplifier system and extends the playback duration. The switchable Class AB/D mode design of the CS83826C minimizes the interference of the power amplifier on FM signals in the audio subsystem, enabling terminal products to achieve ultimate power output performance.

The fully differential architecture and ultra-high PSRR of it effectively enhance its ability to suppress RF noise. The filter-free PWM modulation structure, built-in BOOST voltage boost module, and the proprietary AERC (Adaptive Edge Rate Control) technology adopted by the CS83826C significantly reduce EMI across the entire audio bandwidth. Additionally, the CS83826C integrates over-current protection, short-circuit protection, and over-temperature protection mechanisms, which effectively safeguard the chip from damage under abnormal operating conditions.

Features

- Built-in BOOST Module with Voltage Boosted to 8V, Integrating Both Class AB and Class D Modes
- Output Power
  P_o at 10% THD+N, VIN = 3.7V
  RL = 4Ω+22μH: 2X8W (D MODE NCN OFF)
  P_o at 1% THD+N, VIN = 3.7V
  RL = 4Ω+22μH: 2X6.4W (D MODE NCN OFF)
- Excellent "Pop-Noise" Suppression Capability
- Operating Voltage Range: 2.7V to 5.5V
- Three Adaptive Boost Points to Improve Amplifier Efficiency and Extend Playback Time
- Fixed 50x Gain, Integrated 10K Input Resistor and 500K Feedback Resistor
- Built-in Two Anti-Clipping Modes
- Filter-Free Class-D Architecture
- Maximum Efficiency of 85%(Vbat=4.2V@Po=2x5W)
- High PSRR: 70dB at 217Hz
- Start-up Time: 220ms
- Quiescent Current: 30mA
- Low Shutdown Current: 10μA
- Over-Current Protection, Short-Circuit Protection, and Over-Temperature Protection

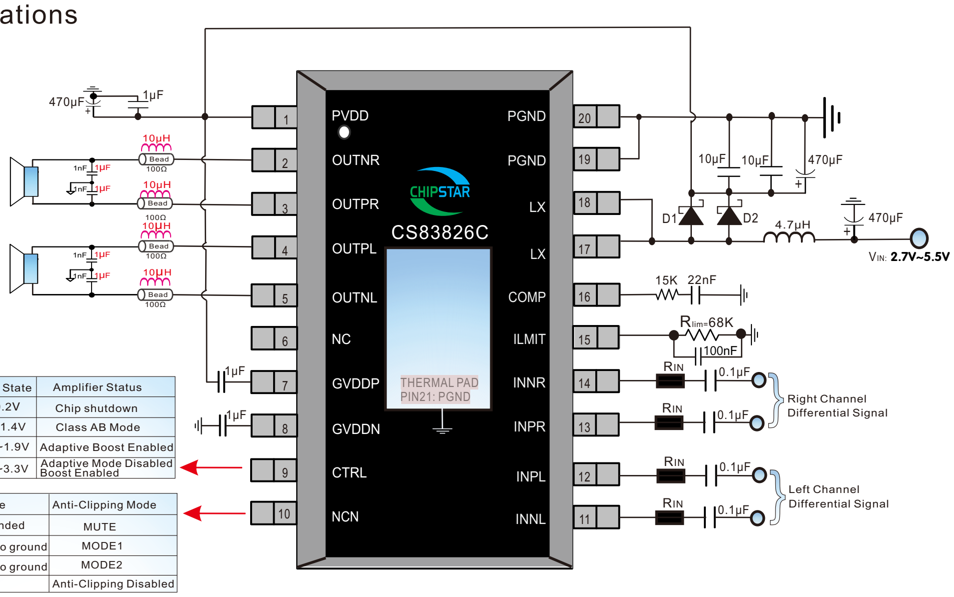
Applications

- Portable Bluetooth Speakers
- Trolley Speakers

Package

- eTSSOP20

Typical Applications



CTRL State	Amplifier Status
0~0.2V	Chip shutdown
1.2~1.4V	Class AB Mode
1.5V~1.9V	Adaptive Boost Enabled
2.2V~3.3V	Adaptive Mode Disabled Boost Enabled

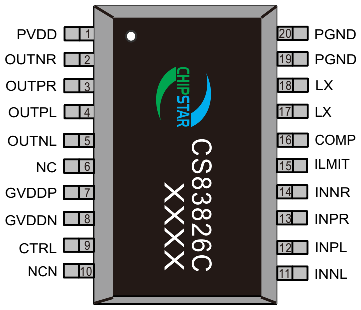
NCN State	Anti-Clipping Mode
Directly Grounded	MUTE
56KΩ connected to ground	MODE1
100KΩ connected to ground	MODE2
Float	Anti-Clipping Disabled

Notes:

- **L1 is an inductor with a value of 4.7uH and a saturation current of 10A or more, and its DCR (Direct Current Resistance) should be sufficiently small. The Schottky diode model for D1 and D2 is SS54.**
- **It features a built–in fixed gain of 50x, integrated with a 10KΩ input resistor and a 500KΩ feedback resistor. The gain calculation formula is: GAIN = 500KΩ/(RIN + 10KΩ)**

PIN Configuration and Functions

CS83826C



eTSSOP20
TOP VIEW

NO.	NAME	I/O	DESCRIPTION	NO.	NAME	I/O	DESCRIPTION
1	PVDD	P	Power Supply Terminal	11	INNL	I	Negative Terminal for Left Channel Audio Signal Input
2	OUTNR	O	Negative Terminal for Right Channel Audio Signal Output	12	INPL	I	Positive Terminal for Left Channel Audio Signal Input
3	OUTPR	O	Positive Terminal for Right Channel Audio Signal Output	13	INPR	I	Positive Terminal for Right Channel Audio Signal Input
4	OUTPL	O	Positive Terminal for Left Channel Audio Signal Output	14	INNR	I	Negative Terminal for Right Channel Audio Signal Input
5	OUTNL	O	Negative Terminal for Left Channel Audio Signal Output	15	LIMIT	I	Inductor Peak Current Limiting Pin
6	NC	-	Empty Pin	16	COMP	I	External Compensation Pin
7	GVDDP	I	Upper Transistor Gate Drive Voltage	17	LX	I	Switching Pin, Connects to External Inductor
8	GVDDN	I	Internal Voltage Regulator	18	LX	I	Switching Pin, Connects to External Inductor
9	CTRL	I	Shutdown, Class AB, Adaptive State Control Pin	19	PGND	-	Power Ground
10	NCN	I	Mute and Anti-Clipping Control Pin	20	PGND	-	Power Ground
				21 (HeatSink)	PGND	-	Power Ground

Absolute Maximum Ratings [1]

SYMBOL	PARAMETER	VALUE	UNIT
VMAX	VIN	-0.3~13	V
T_J	Junction operating temperature range	-40~150	℃
T_{STG}	Storage temperature range	-55~150	℃
T_{SDR}	Lead temperature (Soldering, 10 sec.)	260	℃

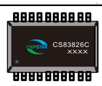
Recommended Operating Conditions

SYMBOL	PARAMETER	VALUE	UNIT
V_{IN}	Input power supply voltage	2.7~5.5	V
T_J	Junction operating temperature range	-40~125	℃
T_A	Ambient temperature range	-40~85	℃

Thermal Information [2]

SYMBOL	PARAMETER	VALUE	UNIT
θ_{JA}	Package thermal resistance - chip to environment thermal resistance	36	℃/W

Ordering Information

Device	Package Type	Device Marking	Reel Size	Tape Width	Quantity
CS83826C	eTSSOP20		13”	16mm	5000

ESD Ratings

HBM (Human Body Model) -- ±2KV

MM (Machine model) -- ±200V

1. The above parameters are merely the limit values for the device's operation. It is not recommended to operate the device beyond these limits; otherwise, it will affect the device's reliability and service life, and may even cause permanent damage.
2.The area on the PCB where the CS83826C is placed requires a heat dissipation design. This design should ensure that the heat sink at the bottom of the CS83826C is connected to the heat dissipation area of the PCB, and is further connected to the ground (GND) via vias.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Test Condition	MIN	TYP	MAX	UNITS
$\lvert V_{OO} \rvert$	Output offset voltage	VIN=0V, Av=2V/V V_{IN}=3.0V to 5.0V		5	25	mV
PSRR	Power Supply Voltage Rejection Ratio	V_{IN}=3V to 5V,217Hz		-70		dB
CMRR	Common Mode Rejection Ratio	Input Pins Shorted , V_{DD} = 3V to 5V		-72		dB
I_{DD}	Quiescent current	VIN=5V, No Load, No Filter		30		mA
I_{SD}	Shutdown current			10		μA
$r_{DS(ON)}$	Conduction Resistance of Power Amplifier Module	V_{IN}= 3.7V		80		mΩ
		V_{IN}=4V		80		
$f_{(SW)}$	Class D Modulation Frequency	V_{IN}=3V to 5V		300		KHz
Rin	Built-in Input Resistor			10		KΩ
Rf	Built-in Feedback Resistor			500		KΩ
V_{IH}	Pins CTRL and NCN input high level				6.0	V
V_{IL}	Pins CTRL and NCN input low level		0.2			V

Electrical Parameters of BOOST Module

(T_A = +25°C, VDD = VEN = 3.7V, unless otherwise specified)

Parameter	Test Condition	MIN	TYP	MAX	UNITS
Input Voltage		2.7		5.5	V
Under-Voltage Protection Threshold	V_{IN} Rising		2.0		V
Switching Frequency			300		KHZ
Maximum Duty Cycle		85			%
Switching Transistor On-State Current	V_{DD}= 3.7V, Duty Cycle= 70%		8.0		A
Switching Transistor On-State Impedance			12		mΩ
Switching Transistor On-State Leakage Current	V_{LX} = 8.7V, EN = 0			15	μA
Over-Temperature Protection Threshold			160		°C
Over-Temperature Protection Hysteresis			40		°C

Operating Characteristics(T_A=25°C, RL = 4Ω+33uH)

Symbol	Parameter	Test Condition	MIN	TYP	MAX	UNITS
P_o	NCNOFF Mode,Output Power (Class D Mode)	Vbat=3.5V,THD=10%,f=1KHz,RL=4 Ω		2x8		W
		Vbat=3.5V,THD=1%,f=1KHz,,RL=4 Ω		2x6.4		
THD+N	Total Harmonic Distortion + Noise	Vbat=3.7V,Po=5W, f=1KHz		0.09		%
η	Efficiency	Vbat=3.7V, f=1KHz,Po=2x3W,RL=4 Ω+33uH		87		%
		Vbat=3.7V,f=1KHz,Po=2x2W,RL=4 Ω+33uH		85		
t_{ST}	Chip Startup Time			220		ms
Vn	Output Noise Floor	Differential input floating,f=20~20K,A-Weighted		100		μV

Operating Characteristics

T_A=25°C, RL = 4Ω, Pure Resistance, Class AB Mode

Symbol	Parameter	Test Condition	MIN	TYP	MAX	UNITS
P_O	Class AB Mode	Vbat=5.0V,THD=10%,f=1KHz,RL=4Ω		2x3		W
		Vbat=4.0V,THD=10%,f=1KHz,RL=4Ω		2x1.9		
		Vbat=5.0V,THD=10%,f=1KHz,RL=3Ω		2x3.75		
		Vbat=4.0V,THD=10%,f=1KHz,RL=3Ω		2x2.35		
THD+N	Total Harmonic Distortion + Noise	Vbat=4.0V,Po=1.0W, f=1KHz,RL=4Ω		0.20		%
		Vbat=3.7V,Po=0.5W, f=1KHz,RL=4Ω		0.20		

T_A = 25°C. Unless otherwise specified, the default RL = 4Ω + 47 μH, operating in Class D Mode, and NCN is grounded through a 56 KΩ resistor.

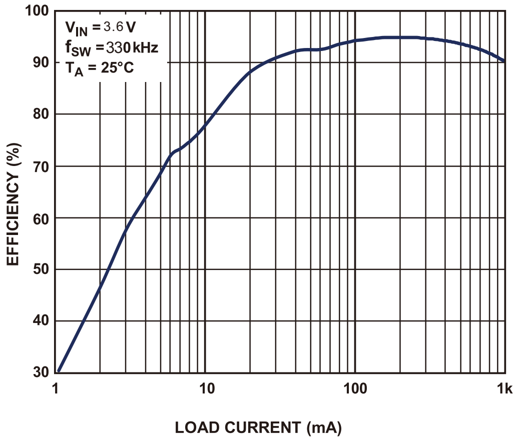
Symbol	Parameter	Test Condition	MIN	TYP	MAX	UNITS
P_O	Output Power	Vbat=3.6V,NCN MODE2,RL = 4 Ω+47uH		2x5.0		W
THD+N	Total Harmonic Distortion + Noise	Vbat=3.6V,NCN MODE2,RL = 4 Ω+47uH		0.9		%
T_{at}	Anti-Distortion Activation Time			4		ms
T_{rl}	Anti-Distortion Release Time			2		s

T_A = 25°C. Unless otherwise specified, the default RL = 4Ω + 47 μH, operating in Class D Mode, and NCN is grounded through a 100 KΩ resistor.

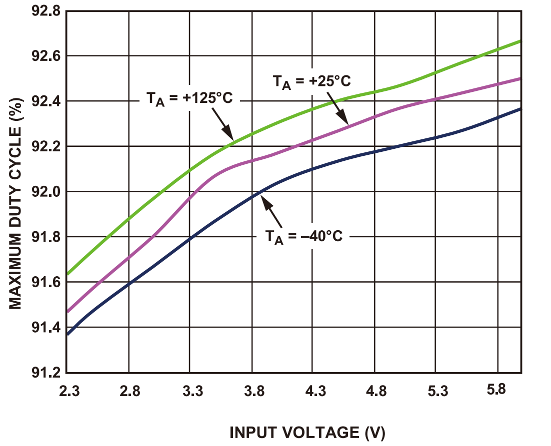
Symbol	Parameter	Test Condition	MIN	TYP	MAX	UNITS
P_O	Output Power	Vbat=3.6V,NCN MODE2,RL = 4 Ω+47uH		2x5.6		W
THD+N	Total Harmonic Distortion + Noise	Vbat=3.6V,NCN MODE2,RL = 4 Ω+47uH		1.2		%
T_{at}	Anti-Distortion Activation Time			50		ms
T_{rl}	Anti-Distortion Release Time			75		ms

Typical Characteristic Curve of the BOOST Module

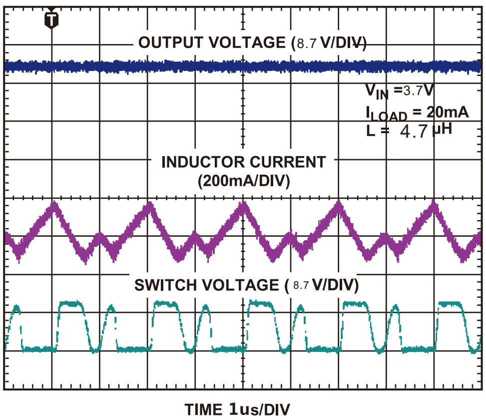
TA=25°C, RL = 4 Ω



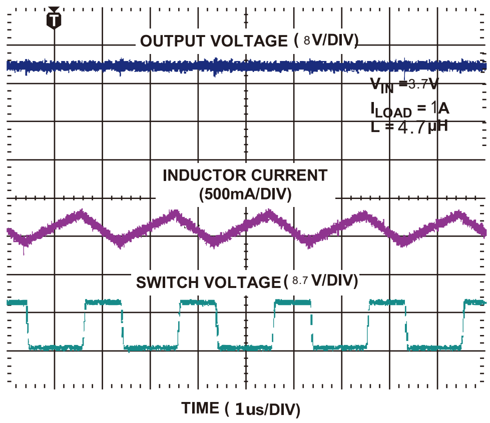
Efficiency vs. Load Current, V_{IN} =7.4 V, f_{SW} = 330KHz



Maximum Duty Cycle vs. Input Voltage, f_{SW} = 330KHz



Switching Waveform in Discontinuous Conduction Mode

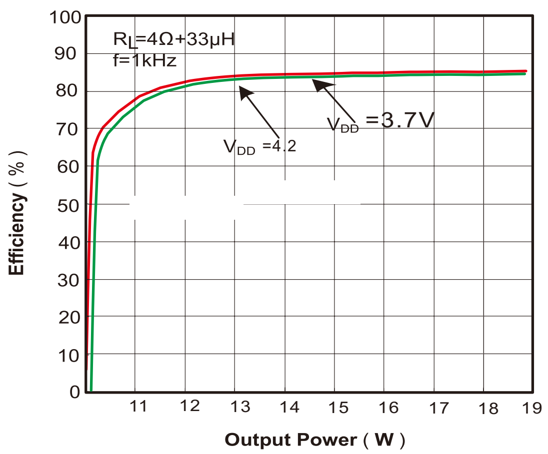


Switching Waveform in Continuous Conduction Mode

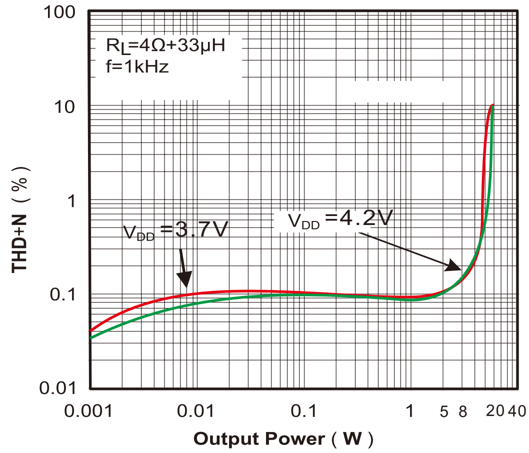
TYPICAL PERFORMANCE CHARACTERISTICS

TA=25°C, RL = 4 Ω ,Class D mode

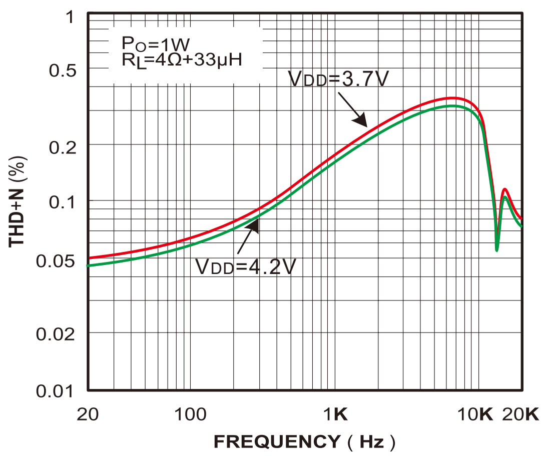
EFFICIENCY vs OUTPUT POWER



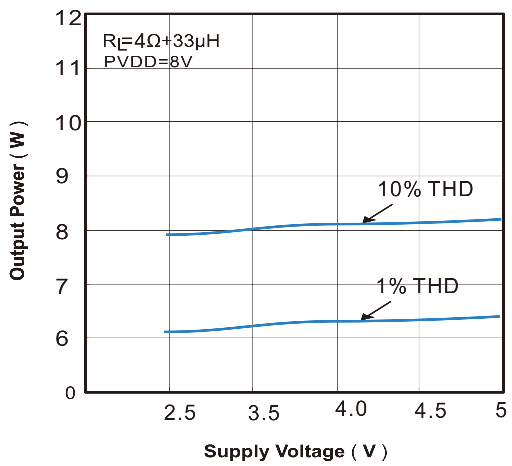
THD+N vs OUTPUT POWER



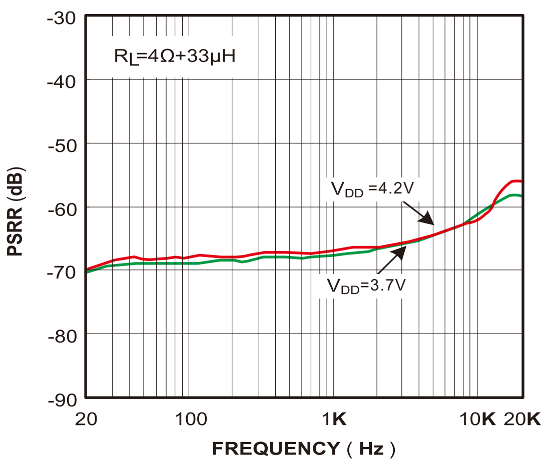
THD+N vs FREQUENCY



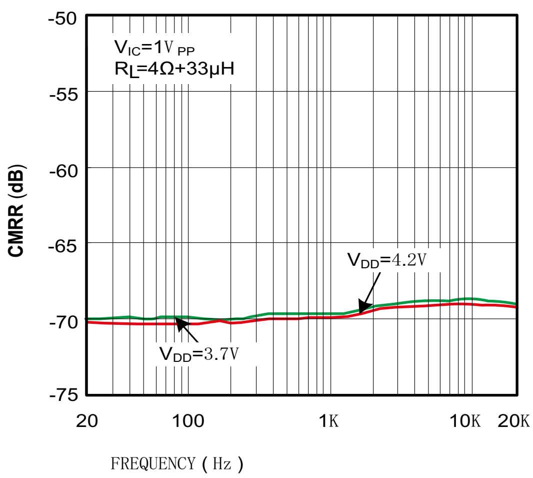
OUTPUT POWER vs SUPPLY VOLTAGE



PSRR vs FREQUENCY



CMRR vs FREQUENCY



CS83826C Application Points

The CS83826C is an R-class stereo audio power amplifier designed for single-cell lithium battery-powered applications. It features fixed gain, two anti-distortion modes, AB/D mode switching, a mute function, and a built-in BOOST step-up module.
When powered by a single-cell lithium battery, the CS83826C can drive speakers with an impedance as low as 4Ω, delivering a maximum constant output power of 2×8W at 10% total harmonic distortion (THD).
It is equipped with three adaptive step-up points; based on the input audio signal amplitude, the amplifier automatically selects the appropriate step-up point. This optimization maximizes the efficiency of the power amplifier system and extends the playback duration of the amplifier.
The AB-class/D-class switchable design of the CS83826C minimizes the interference of the power amplifier on FM signals in the audio subsystem, providing terminal products with extreme power output performance. Additionally, the CS83826C adopts a fully differential architecture and boasts an ultra-high power supply rejection ratio (PSRR), which effectively enhances its ability to suppress RF noise.
Its filterless PWM modulation structure, integrated BOOST step-up module, and proprietary Adaptive Edge Rate Control (AERC) technology significantly reduce EMI interference across the entire audio bandwidth. Furthermore, the CS83826C incorporates built-in overcurrent protection, short-circuit protection, and over-temperature protection, which effectively safeguard the chip from damage under abnormal operating conditions.

Pop & Click Suppression

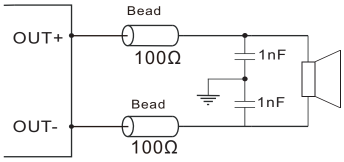
The CS83826C integrates a proprietary timing control circuit to achieve comprehensive Pop&Click suppression, which can effectively eliminate transient noise that may occur in the system during power-on, power-off, wake-up, and shutdown operations.

Protection Circuits

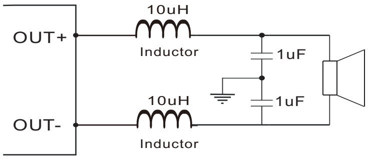
During the application of the CS83826C, if the chip experiences faults such as short circuits between the output pins and the power supply or ground, or short circuits between outputs, the overcurrent protection circuit will shut down the chip to prevent damage. After the short-circuit fault is eliminated, the CS83826C will automatically resume operation.
When the chip temperature is too high, the chip will also shut down. Once the temperature drops, the CS83826C can continue to work normally. In addition, when the power supply voltage is too low, the chip will be shut down as well; after the power supply voltage is restored, the chip will start up again.

Inductors, Ferrite Beads, and Capacitors

The CS83826C module can pass FCC Class B testing under various conditions (such as high power and long output load lines) when tested with a ferrite bead filter. The type and specifications of the ferrite bead can be selected based on actual application requirements. As shown in the figure below:



If the amplifier is used in a system with strict noise requirements, an LC filter can be considered for series connection at the output. The relevant parameters of the filter are shown in the figure below:



Schottky Diode

The BOOST section of the CS83826C adopts asynchronous rectification and requires an external Schottky diode for freewheeling. The Schottky diode has a significant impact on the overall performance of the IC; improper selection may lead to low efficiency of the entire system, or even generate a large reverse overshoot voltage at the IC's LX pin, resulting in IC burnout.
We recommend using two 40V Schottky diodes (e.g., SS54). It is important to note that the wiring from the Schottky diode to the inductor, then to the output filter capacitor, and finally to the PVDD pin should be as short as possible. Improper wiring will increase the overshoot and ringing at the LX pin, affecting EMI performance and even causing IC burnout.

Selection of Inductor

The inductor has a significant impact on the performance of the CS83826C. Based on considerations such as ripple stability, it is recommended to use an inductor for L1 with the following specifications: inductance of 4.7μH and saturation current of 10A or more. Additionally, the DC resistance (DCR) of the selected inductor should be sufficiently low.

Efficiency

The high efficiency of the Class R amplifier is determined by the switching operation mode of the output transistors. In a Class R amplifier, the output transistors act like current-adjusting switches, and the additional power consumed during the switching process is basically negligible. The power loss related to the output stage is mainly the IR drop generated by the MOSFET on-resistance and the power supply current. After the BOOST circuit starts up, the efficiency of the CS83826C can reach 85%.

Amplification Gain

The CS83826C integrates an input resistor of 10KΩ and a feedback resistor of 500KΩ, allowing the setting of a reasonable amplification gain for the audio subsystem. The formula for calculating the gain of the CS83826C is: Gain = 500 KΩ/RIN + 10KΩ.

Input Capacitor

A high-pass filter is formed by the input resistor and the input capacitor, with its cutoff frequency calculated by the following formula:

$$f_c = \frac{1}{2\pi(Ri+10K)Cin}$$

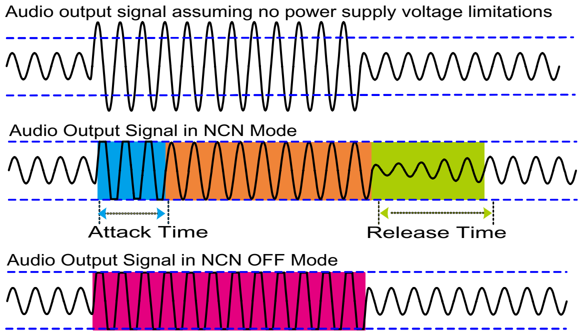
The value of the input capacitor is of great importance, as it is generally considered to directly affect the low-frequency performance of the circuit. Speakers in wireless telephones usually cannot respond well to low-frequency signals; therefore, a relatively large fc (cutoff frequency) can be selected in the application to filter out interference caused by 217Hz noise. Good matching between capacitors helps improve the overall performance of the chip and the suppression of Pop & Click noise. Thus, it is required to select capacitors with a tolerance of 10% or less.

NCN Function

In audio applications, factors such as excessively large input signals or decreasing battery voltage can cause the output signal of the audio power amplifier to suffer from distortion (commonly referred to as "clipping"). Furthermore, overloaded signals can cause permanent damage to the speaker. The CS83826 features a unique No Clipping Noise (NCN) function: by detecting clipping distortion in the amplifier's output signal, it automatically adjusts the system gain to keep the output audio signal smooth and rounded. This not only effectively prevents damage to the speaker caused by high-power overload output but also provides a more comfortable listening experience.

The CS83826C offers five user-selectable operating modes related to NCN, including a non-anti-clipping mode and a MUTE function: MUTE, M1, M2, and NCN OFF. These five modes can be accessed by setting different states of the NCNL and NCNR pins respectively.

NCN State	Anti-Clipping Mode	Attack Time	Release Time
Directly Grounded	MUTE		
56KΩ connected to ground	MODE1	4ms	2s
100KΩ connected to ground	MODE2	50ms	75ms
Float	Anti-Clipping Disabled		



Current Limiting Function

By connecting a pull-down resistor from the ILIMIT pin to ground, the peak current of the BOOST inductor can be limited, and the power supply soft-start function can be implemented. The table below lists the soft-start time and the effective value of the inductor current under different resistor and capacitor conditions for reference.

Inductor	Rlim	Power Supply Soft-Start Time			Effective Value of Inductor Current
		10nF	100nF	220nF	
4.7uH	68K	2ms	19ms	41ms	6.5A
	75K	2.2ms	21ms	46ms	8.0A

CTRL Operating Mode Settings

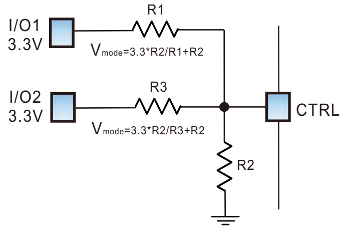
The CS83826C has four operating modes: chip shutdown, Class AB mode, adaptive boost enable, and boost enable + adaptive disable. Switching between these modes can be achieved through simple hardware settings on the CTRL pin.

CTRL State	Amplifier Status
0~0.2V	Chip shutdown
1.2~1.4V	Class AB Mode
1.5V~1.9V	Adaptive Boost Enabled
2.2V~3.3V	Adaptive Mode Disabled Boost Enabled

IO Settings for the Four Operating Modes

Based on the Control Method in the Above Table, the Following Settings Can Be Made According to the System in Practical Use:

If the IO control voltage of the main controller is 3.3V, as shown in the figure, four operating states can be switched using two IO ports and a voltage divider circuit:



- When both IO1 and IO2 are at low level, the CS83826C enters shutdown mode.

- When IO1 is at high level and IO2 is floating, the CS83826C enters Class AB mode as long as the appropriate resistance ratio of R1 and R2 is selected to keep the VCTRL voltage between 1.2V and 1.4V.
- When the appropriate resistance ratio of R1 and R2 is selected to keep the VCTRL voltage between 1.5V and 1.9V, the CS83826C enters the boost enable + adaptive enable mode.
- When IO1 is floating and IO2 is at high level, the CS83826C enters the boost enable + adaptive disable mode as long as the appropriate resistance ratio of R3 and R2 is selected to keep the VCTRL voltage above 2.2V.

The absolute values of R1, R2, and R3 are determined by the acceptable power consumption, and the CTRL pin itself does not require a drive current.

Adaptive Boost Function

The CS83826C is equipped with a real-time audio-tracking boost function. It automatically selects the boost voltage (5V, 6V, up to a maximum of 8V) based on the output power of the audio signal. This effectively reduces the boost ratio and maintains the system at peak efficiency throughout the playback process. As a result, the system efficiency is significantly improved, which in turn substantially extends the system's playback duration.

PCB Board Design Steps and Key Points for CS83826C

Vbat Pin Capacitors

The CS83826C integrates a voltage regulation circuit internally. Therefore, there is no need to power the CS83826C through Vbat, and consequently, no surface-mount decoupling capacitor is required—you can directly connect the inductor to Vbat. However, we generally recommend adding at least one energy-storage electrolytic capacitor to Vbat, as both the boost power supply and the power amplifier draw current from Vbat. A 470μF electrolytic capacitor helps stabilize the battery voltage, reduces interference to other ICs in the system, improves the low-frequency transient response of the CS83826C, and contributes to the reduction of EMI.

PVDD Pin Capacitors

The PVDD pin of the CS83826C actually serves as the output of the boost power supply and also the power input for the built-in power amplifier module. Therefore, filter and decoupling capacitors are mandatory. We require the use of two sets of capacitors:

One set consists of a 10μF decoupling capacitor and a 470μF filter electrolytic capacitor. These should be placed as close to the Schottky diode as possible.

The other set, composed of a 1μF surface-mount capacitor and a 10 μF surface-mount capacitor, should be placed as close to the chip pins as possible.

The 470μF filter capacitor is also mandatory (it is recommended to use high-frequency, low-impedance series electrolytic capacitors, which can effectively improve efficiency and reduce voltage ripple). An excessively small capacitor will cause oscillation in the output voltage of the BOOST module. The PVDD pin capacitors have a significant impact on the performance of the CS83826C. For specific details, please refer to the PCB design guidelines or contact the original manufacturer's engineers.

Chip GND (PGND)

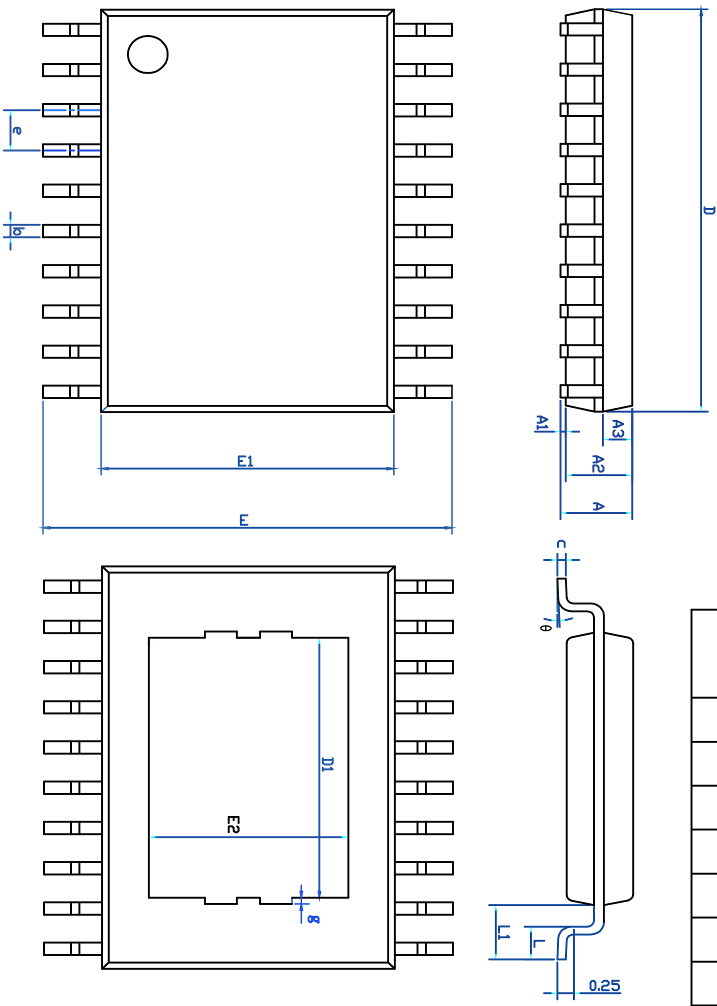
PGND is the power ground. Transient currents exceeding 10A may flow through it, and it also functions as the chip's heat sink. It must be directly connected to the copper pour, and a sufficient number of vias must be used to connect it to the bottom-layer copper pour.

Input Audio GND

The CS83826C features differential input. When the audio source also has differential output, the CS83826C can effectively shield interference, and there is no need to worry excessively about the introduction of ground loop noise. However, when the audio source has single-ended output, attention must be paid to shielding against the introduction of ground loop noise. Since the characteristics of each system, main controller, or DAC vary, we can generally only recommend ensuring that there is no potential difference between the reference ground of the audio signal and the reference ground of the CS83826C's pin (which is grounded via a capacitor with no signal input), or that they are ideally the same ground.

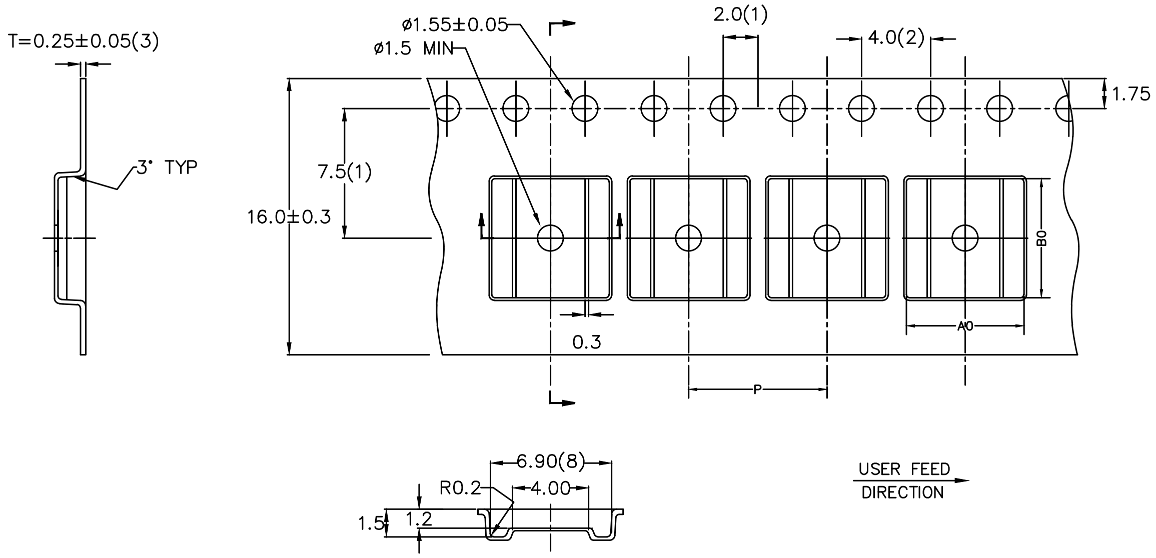
Package Information

CS83826C eTSSOP20 (Units:mm)



SYMBOL	MI LLIMETER		
	MIN	NOM	MAX
A	——	——	1. 20
A1	0. 04	0. 08	0. 12
A2	0. 95	1. 00	1. 05
A3	0. 39	0. 44	0. 49
b	0. 20	——	0. 29
c	0. 13	——	0. 18
D	6. 40	6. 50	6. 60
D1	4. 10REF		
E	6. 30	6. 40	6. 50
E1	4. 30	4. 40	4. 50
E2	2. 90REF		
e	0. 65BSC		
L	0. 50	0. 60	0. 70
L1	1. 00REF		
θ	0°	——	8°
g	0. 10REF		

TAPE AND REEL INFORMATION



A0	B0	K0	P	P0	E	F	D0	P2	T	W
6.65±0.1	6.80±0,1	1.5±0.1	8.0±0.1	4.0±0.1	1.75±0.1	7.5±0.1	1.55±0.05	2.0±0.1	0.25±0.05	16±0.3

NOTES:
1. MEASURED FROM THE CENTERLINE OF SPROCKET HOLE TO CENTERLINE OF THE POCKET HOLE AND FROM THE CENTERLINE OF SPROCKET HOLE TO CENTERLINE OF THE POCKET
2. CUMULATIVE TOLERANCE OF 10 SPROCKET HOLES IS ±0.20
3. THIS THICKNESS IS APPLICABLE AS MEASURED AT THE EDGE OF THE TAPE
4. MATERIAL: CONDUCTIVE POLYSTYRENE
5. DIM IN MM
6. ALLOWABLE CAMBER TO BE 1mm PER 100mm IN LENGTH, NON-CUMULATIVE OVER 250mm
7. UNLESS OTHERWISE SPECIFIED, TOLERANCE ±0.10
8. MEASUREMENT POINT TO BE 0.3 FROM BOTTOM POCKET .
9. SURFACE RESISTIVITY LESS THAN OR EQUAL TO 1.0X10E6 OHMS/SQUARE .

Precautions for MOS Circuit Operation:

Static electricity can be generated in many places. The following precautions can effectively prevent MOS circuit from being damaged due to the sound of electrostatic discharge:

- Operators shall be grounded through anti-static wrist strap.
- The equipment enclosure must be grounded.
- Tools used during assembly must be grounded.
- Conductor packaging or anti-static materials must be used for packaging or transportation.

Declaration:
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