Built-in Adaptive Boost Module, Anti-clipping, AB/D Mode Switching 17W Output Power Class R Mono Audio Power Amplifier

General Description

The CS83722E is a Class R audio power amplifier with a built-in BOOST boost module and anti-clipping function. It can deliver a constant maximum power of 17W into a 3Ω load. Adopting switchable Class AB/Class D mode design, it minimizes the interference of the power amplifier on FM within the audio subsystem. Operating within the supply voltage range of lithium batteries, the CS83722E delivers extreme power output performance, making it an optimal choice for portable speaker devices, especially megaphone products.The fully differential architecture and ultra-high PSRR of the CS83722E effectively enhance its capability to suppress RF noise. Equipped with proprietary AERC (Adaptive Edge Rate Control) technology, the device drastically reduces EMI interference across the full audio bandwidth. For a 60 cm audio cable, it achieves a margin of more than 20dB under FCC standards.

In addition, the CS83722E integrates over-current protection, short-circuit protection and over-temperature protection, which effectively safeguard the chip from damage under abnormal operating conditions.The CS83722E is available in a compact ESOP10L package for customer selection, with a rated operating temperature range from -20℃ to 85℃.

Features

- Built-in BOOST module with Class R architecture, integrated switchable Class D / Class AB dual modes
- Output Power (D MODE, NCN OFF)
  VIN=3.7V, RL=3Ω+33μH
  PO=17W @ 10% THD+N PO=14W @ 1% THD+N
  VIN=3.7V, RL=4Ω+33μH
  PO=13.5W @ 10% THD+N PO=11W @ 1% THD+N
- Excellent pop-noise suppression performance
- Operating voltage range: 2.7V ~ 5.5V
- SD pin supports one-wire pulse width control mode, and voltage divider resistor control mode
- Built-in fixed gain of 50 times; BOOST boost up to 10V
- Advanced power adaptive function
- Built-in anti-clipping module
- Filterless Class-D architecture
- Peak efficiency up to 82%
- High PSRR: 70dB @ 217Hz
- Turn-on time: 100ms
- Quiescent current: 8mA
- Low shutdown current: < 10μA
- Over-current protection, short-circuit protection and over-temperature protection
- RoHS-compliant lead-free package

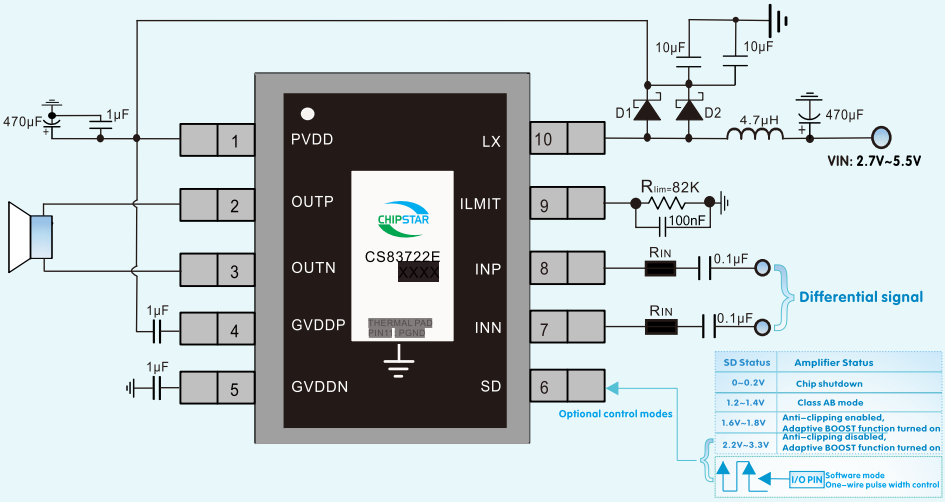
Package

- ESOP10L

Applications

- Portable Bluetooth Speaker

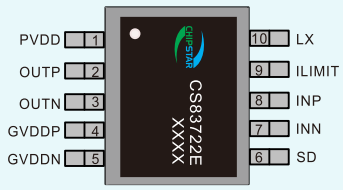
Typical Applications

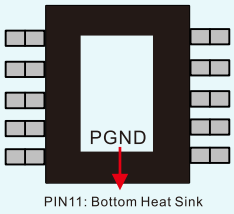


Note:

- Schottky diodes D1 and D2 adopt model SS34.
- The CS83722E features a fixed internal gain of 50 times, with an integrated input resistance of 10K and feedback resistance of 500K.Gain calculation formula:GAIN=500K/RIN+10K
- The bottom thermal pad of CS83722E is defined as the PGND pin.
- The SD pin is controlled by voltage divider resistors. The adaptive BOOST function of CS83722E is enabled by default.

PIN Configuration and Functions





PIN11: Bottom Heat Sink

NO.	NAME	I/O	DESCRIPTION
1	PVDD	P	Power Supply
2	OUTP	O	Non-inverting audio output
3	OUTN	O	Inverting audio output
4	GVDDP	I	Upper tube gate drive voltage
5	GVDDN	I	Internal voltage regulator
6	SD	I	Shutdown, Class AB, anti-clipping, adaptive mode control pin, available for one-wire PWM control
7	INN	I	Audio input negative terminal
8	INP	I	Audio input positive terminal
9	ILIMIT	I	Inductor peak current limit pin
10	LX	I	Switch pin, connect external inductor
11 Thermal PAD	PGND	-	Power GND

Absolute Maximum Ratings [1]

SYMBOL	PARAMETER	VALUE	UNIT
VMAX	ILIMIT,LX, OUTN,OUTP, GVDDP, GVDDN	-0.3~13	V
	SD,INN,INP	-0.3~6	V
T_J	Junction operating temperature range	-40~150	℃
T_{STG}	Storage temperature range	-55~150	℃
T_{SDR}	Lead temperature (Soldering, 10 sec.)	260	℃

Recommended Operating Conditions

SYMBOL	PARAMETER	VALUE	UNIT
V_{IN}	Input power supply voltage	2.7~5.5	V
T_J	Junction operating temperature range	-40~125	℃
T_A	Ambient temperature range	-40~85	℃

Thermal Information [2]

SYMBOL	PARAMETER	VALUE	UNIT
θ_{JA}	Package thermal resistance - chip to environment thermal resistance	50	℃/W
θ_{JC}	Package thermal resistance - chip to Package Surface Thermal Resistance	10	℃/W

Ordering Information

Device	Package Type	Device Marking	Package size	Tape Width	Quantity
CS83722E	ESOP10L		13”	12mm	4000 units

ESD Ratings

HBM (Human Body Model) ---------- ±4KV

MM (Machine model) ---------- ±400V

1. The above parameters are only the limit values of device operation. It is not recommended that the working conditions of the device exceed the limit values. Otherwise, the reliability and life of the device will be affected, and even permanent damage will be caused.
2. Where the PCB board is placed in CS83722E, a heat dissipation design is needed. The heat sink at the bottom of CS83722E is connected with the heat sink area of PCB board.

Electrical Characteristics (T_A=25℃ , unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage	VIN=0V, Av=2V/V VIN=3.0V to 5.0V		5	25	mV
PSRR	Power supply ripple rejection ratio	VIN=3V to 5V,217Hz		-70		dB
CMRR	Common mode rejection ratio	Input pins are shorted together V_{DD} = 3V to 5V		-72		dB
I_{DD}	Quiescent current	VIN=5V,No load, No filter		8		mA
I_{SD}	Turn off current			10		μA
$r_{DS(ON)}$	On resistance of power amplifier module	VIN= 3.7V		80		mΩ
		VIN=4V		80		
$f_{(SW)}$	Class D modulation frequency	VIN=3V to 5V		300		KHz
Rin	Built-in input resistor			10		KΩ
Rf	Built-in feedback resistor			500		KΩ
VIH	Pin Ctrl, NCN input high level				6.0	V
VIL	Pin Ctrl, NCN input low level		0.2			V

Electrical Parameters of BOOST Module (T_A=25℃, VDD = VEN = 3.7V, unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage		2.7		5.5	V
Under voltage protection threshold	V_{IN} Rising		2.0		V
switching frequency			300		KHZ
Maximum duty cycle		85			%
On current of switch tube	V_{DD}= 3.7V, Duty cycle= 70%		8.0		A
On resistance of switch tube			12		mΩ
Conduction leakage current of switch tube	V_{LX} = 8.7V, EN = 0			15	uA
Thermal protection temperature			160		°C
Thermal protection hysteresis			40		°C

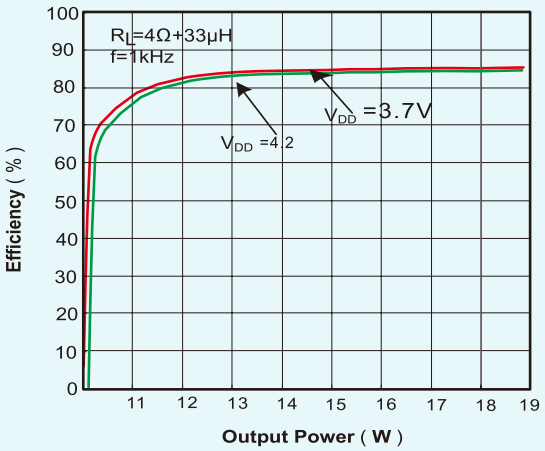
Working characteristics T_A=25°C, RL = 4 Ω+33uH

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PO	NCNOFF Class D Mode Output Power	Vbat=3.7V,THD=10%,f=1KHz,RL=3 Ω		17		W
		Vbat=3.7V,THD=1%,f=1KHz,,RL=3 Ω		14		
		Vbat=3.7V,THD=10%,f=1KHz,RL=4 Ω		13.5		
		Vbat=3.7V,THD=1%,f=1KHz,RL=4Ω		11.0		
	NCNON Class D Mode Output Power	Vbat=3.7V, f=1KHz,,RL=3 Ω		13.4		
		Vbat=3.7V, f=1KHz,RL=4 Ω		10.7		
	Class AB Mode Output Power	Vbat=5.0V,THD=10%,f=1KHz,RL=3 Ω		3.8		
		Vbat=5.0V,THD=10%,f=1KHz,RL=4 Ω		3.0		
THD+N	Total harmonic distortion + noise	Vbat=3.7V,Po=5W, f=1KHz		0.09		%
η	efficiency	Vbat=3.7V, f=1KHz,Po=50W,RL=4 Ω+33uH		82		%
		Vbat=3.7V,f=1KHz,Po=10W,RL=3 Ω+33uH		80		
tST	Chip start time			100		ms
Vn	Output background noise	Differential input floating,f=20~20K,A-Weighted		100		uV

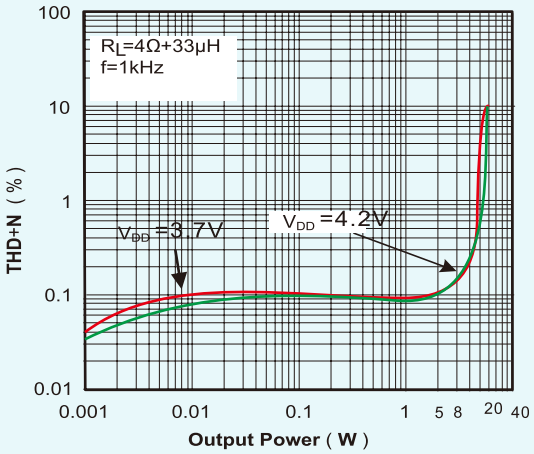
Typical Characteristics

TA=25°C, RL = 4 Ω ,Class D Mode

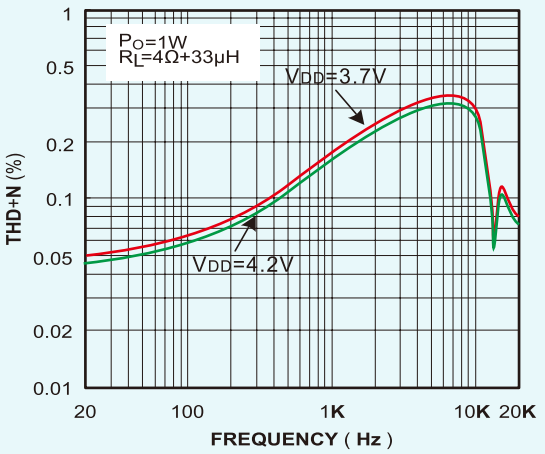
EFFICIENCY vs OUTPUT POWER



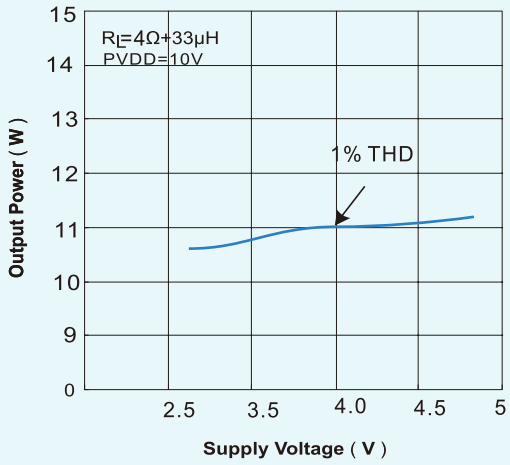
THD+N vs OUTPUT POWER



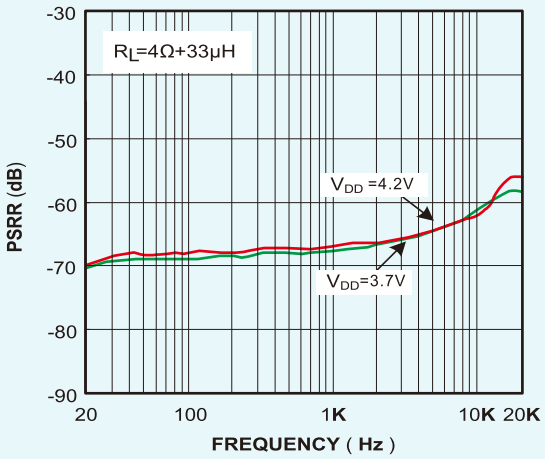
THD+N vs FREQUENCY



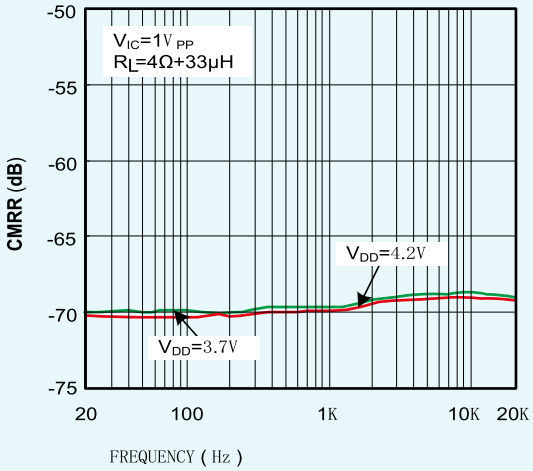
OUTPUT POWER vs SUPPLY VOLTAGE



PSRR vs FREQUENCY



CMRR vs FREQUENCY



CS83722E Application Points

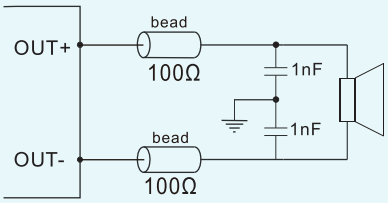
The CS83722E is a Class R stereo audio power amplifier designed for single-cell lithium battery powered applications. It features fixed gain, anti-clipping mode, Class AB/Class D mode switching, and a built-in adaptive BOOST boost module.Powered by a single lithium battery, the CS83722E can drive speakers with impedance as low as 3Ω and deliver a constant maximum output power of 17W. Equipped with an adaptive boost threshold, it automatically enables or disables boost operation according to audio signal amplitude, maximizing system efficiency and extending playback duration.Its switchable Class AB/Class D design greatly minimizes power amplifier interference to FM signals in audio subsystems, delivering superior power output performance for end products. Featuring a fully differential architecture and high PSRR, it achieves excellent suppression of RF noise.Adopting proprietary AERC (Adaptive Edge Rate Control) technology, the device effectively reduces EMI interference across the full audio bandwidth. It also integrates over-current protection, short-circuit protection and over-temperature protection, ensuring reliable chip operation and preventing damage under abnormal working conditions.

Pop & Click Suppression

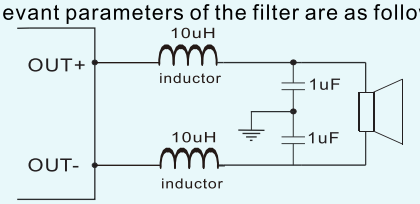
CS83722E has built-in special timing control circuit to achieve comprehensive pop & click suppression, which can effectively eliminate the transient noise that may appear when the system is powered on, down, wake up and shut down.

Inductors, Beads and Capacitors

The CS83722E module can pass the B-level test of FCC under various conditions such as high power and long output load line. The types and specifications of magnetic beads can be selected according to the actual use. As shown in the figure below:



If the amplifier is used in the system with strict noise requirements, the output LC filter can be considered. The relevant parameters of the filter are as follows:



Schottky Diode

The BOOST section of CS83722E adopts non-synchronous rectification, requiring an external Schottky diode for freewheeling. Schottky diodes greatly affect the overall performance of the IC. Improper selection may lead to low system efficiency, and even generate severe reverse overshoot voltage at the IC LX pin, resulting in chip burnout.We recommend using two 40V Schottky diodes such as Ss34. It should be noted that the connection from Schottky to inductor to output filter capacitor to PVDD terminal should be as short as possible. Improper wiring will increase the overshoot ringing at LX terminal, affect EMI and even burn IC.

Selection of Inductor

The inductor has a great influence on the performance of CS83722E. According to the ripple stability and other considerations, it is recommended to use the inductor with L1 of 4.7uh and saturation current of more than 10A. In addition, the selected inductor DCR is small enough.

Efficiency

The switching mode of output transistor determines the high efficiency of class R amplifier. In class R amplifier, the output transistor is like a current adjusting switch, and the extra power consumed in the switching process can be ignored. The output stage related power loss is mainly caused by the IR generated by MOSFET on resistance and supply current. The efficiency of CS83722E can reach 82% after boost start.

Gain

CS83722E has built-in feedback resistor of 500K and built-in input resistor of 10K. We can set reasonable amplification factor of audio subsystem. The calculation formula of CS83722E gain is: gain = 500K / (Rin + 10K).

Input Capacitance

A high pass filter is formed between the input resistor and the input capacitor, and its cut-off frequency is as follows:

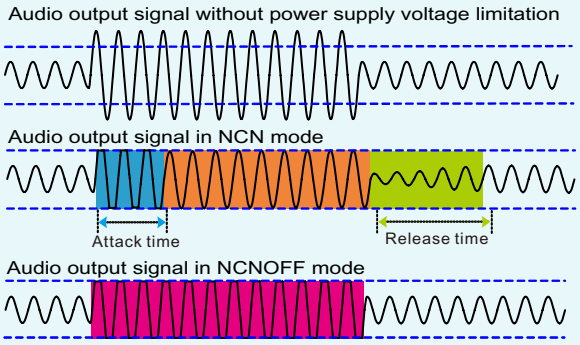
$$f_c = \frac{1}{2\pi(Ri+10K)Cin}$$

The value of input capacitance is very important. It is generally considered that it directly affects the low frequency performance of the circuit. The speaker in the wireless telephone usually can't respond well to the low frequency signal, so we can select a larger FC in the application to filter the interference caused by 217Hz noise. Good matching between capacitors is helpful to improve the overall performance of the chip and pop&click suppression, so it is required to select capacitors with accuracy of 10% or less.

NCN Function

In audio applications, excessive input signals or dropping battery voltage will cause clipping distortion at

the output of audio power amplifiers. Meanwhile, overloaded signals may result in permanent damage to speakers.Featuring exclusive No-Clipping Noise (NCN) function, CS83722E detects output clipping distortion and automatically adjusts system gain to deliver smooth and mellow audio output. It effectively prevents speaker damage caused by high-power overload output and brings superior listening experience.



Current Limiting Function

Set a pull-down resistor from the ILIMIT pin to ground to limit the peak current of the BOOST inductor and realize the power soft-start function. The table below lists the soft-start time and effective inductor current under different resistance and capacitance conditions for reference.

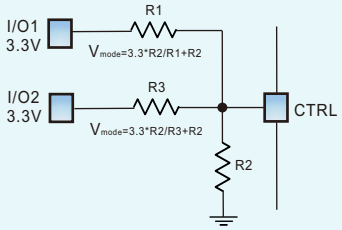
Inductance	Rlim	Power soft start time			Effective value of inductor current
		10nF C	100nF C	220nF C	
4.7μH	68K	2ms	19ms	41ms	5.0A
	82K	2.2ms	21ms	46ms	7.0A

SD Pin Operation Mode Setting

The SD pin of CS83722E can be controlled in two ways: voltage setting via divider resistors and one-wire PWM control. The control methods of the two modes are described as follows:

(1) Divider Resistor Control Method

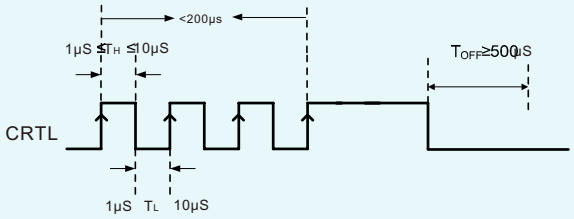
When the main controller IO control voltage is 3.3V, two IO ports and voltage divider circuits can be used to switch operating states as shown in the figure.When both IO1 and IO2 are low level, CS83722E enters shutdown mode.When IO1 is high level and IO2 is floating, select proper resistance ratio of R1 and R2 to make VSD between 1.2V~1.4V, then CS83722E works in Class AB mode.Adjust R1 and R2 ratio to set VSD within 1.6V~1.8V, the chip enables adaptive boost and anti-clipping function simultaneously.When IO1 is floating and IO2 is high level, set proper R3 and R2 ratio to make VSD higher than 2.2V, CS83722E enters the mode with anti-clipping disabled and adaptive boost enabled.The absolute resistance values of R1, R2 and R3 are determined by acceptable power consumption. No driving current is required for the SD pin itself.

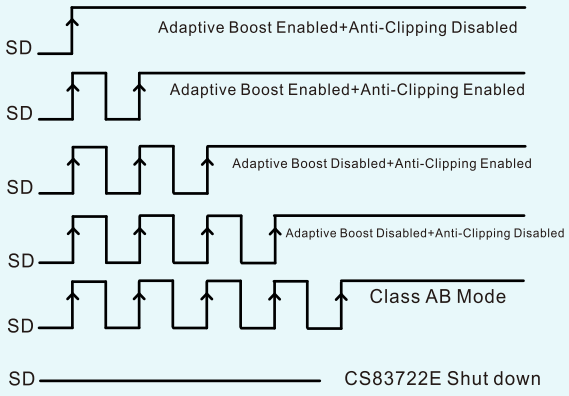


SD Status	Amplifier Status
0~0.2V	Chip shutdown
1.2~1.4V	Class AB mode
1.6V~1.8V	Anti-clipping enabled, Adaptive BOOST function turned on
2.2V~3.3V	Anti-clipping disabled, Adaptive BOOST function turned on

(2) One-Wire PWM Control Mode

The CS83722E also supports one-wire PWM control, which saves one IO port and optimizes system resource utilization. The operating mode of the chip is determined by the number of rising edges of the one-wire pulse signal input to the SD pin, as shown in the figure below.Pull the SD pin high directly (1 rising edge): the chip enters the mode with adaptive boost enabled and anti-clipping disabled.Apply high-low-high pulse signal to the CTRL pin (2 rising edges): the chip enters the mode with both adaptive boost and anti-clipping enabled.3 rising edges received by SD pin: adaptive boost disabled, anti-clipping enabled.4 rising edges received by SD pin: both adaptive boost and anti-clipping disabled.5 rising edges received by SD pin: the chip switches to Class AB mode.The total duration for sending pulse signals to CS83722E shall be less than 200μs. After a typical interval of 1ms, the pulse receiving circuit will be locked. To transmit new pulses again, pull the SD pin low for more than 500μs in advance.Pull the SD control signal low and keep the level for at least 500μs, and the chip will enter shutdown mode.In the timing diagram of one-wire pulse signal:TH: High-level pulse width, recommended value: 2μsTL: Low-level pulse width, recommended value: 2μsTOFF: Minimum low-level duration required for the chip to enter shutdown mode





One-wire Pulse Signal Timing Diagram

Adaptive Boost Function

The CS83722E features real-time audio tracking boost function. It automatically switches the boost output between 5V and 10V according to actual audio output power. This keeps the system operating at optimal efficiency during playback and effectively extends audio playing time.

CS83722E PCB Design Procedures and Key Points

Capacitors at Vbat Terminal

The CS83722E integrates an internal voltage regulator, so it does not need power supply from the Vbat pin, and no SMD decoupling capacitor is required here. It can be directly connected to the inductor. Nevertheless, it is recommended to fit at least one energy-storage electrolytic capacitor on Vbat. Since both the boost power supply and power amplifier draw current from Vbat, a 470μF electrolytic capacitor can stabilize battery voltage, reduce interference to other ICs in the system, improve low-frequency transient response of CS83722E and lower EMI level.

Capacitors at PVDD Terminal

PVDD is the output of the internal boost converter and also serves as the power supply input for the built-in power amplifier block. Hence filter and decoupling capacitors are mandatory.Two sets of capacitors are required:One set consists of a 10μF decoupling capacitor and a 470μF electrolytic filter capacitor, which shall be placed as close to the Schottky diode as possible.The other set including 1μF and 10μF SMD capacitors shall be placed nearest to the IC pins.The 470μF filter capacitor is essential. High-frequency low-impedance electrolytic capacitors are recommended to boost efficiency and suppress voltage ripple. Insufficient capacitance will cause output voltage oscillation of the BOOST module. Capacitors at PVDD greatly affect the overall performance of CS83722E. Refer to the official PCB design guideline or contact factory technical engineers for details.

IC Ground Layout

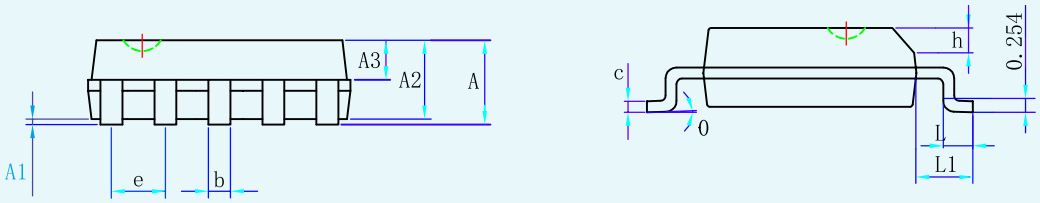
PGND is the power ground, where instantaneous current can exceed 10A, and it also acts as the chip thermal pad. It must be directly connected to copper plane, with sufficient thermal vias linking to the bottom-layer copper area.

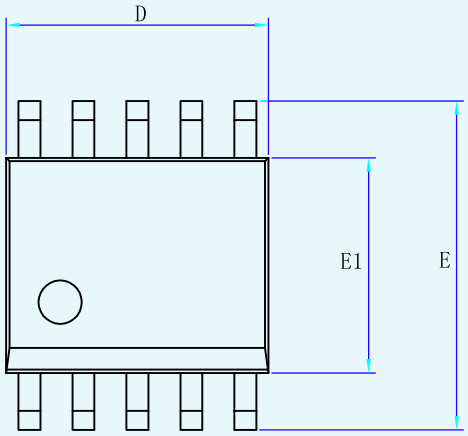
Audio Input Ground

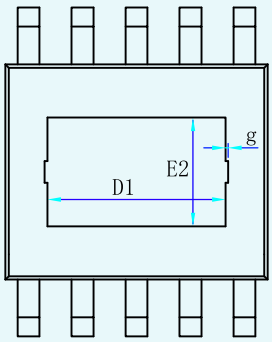
CS83722E adopts differential input architecture. When matched with differential-output audio sources, it features excellent anti-interference capability with negligible ground loop noise impact.While connecting to single-ended audio sources, measures must be taken to restrain ground loop noise.Given the varied characteristics of main controllers and DACs in different systems, it is advised to eliminate potential potential difference between the reference ground of audio signals and the ground reference of CS83722E signal input pins with grounded capacitors, or unify them into the same ground plane as much as possible.

Package Information

CS83722E ESOP10L





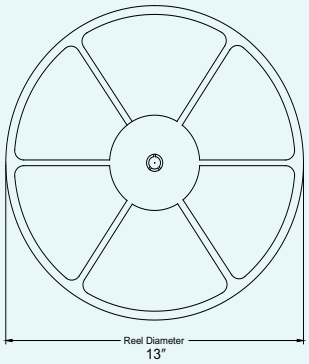


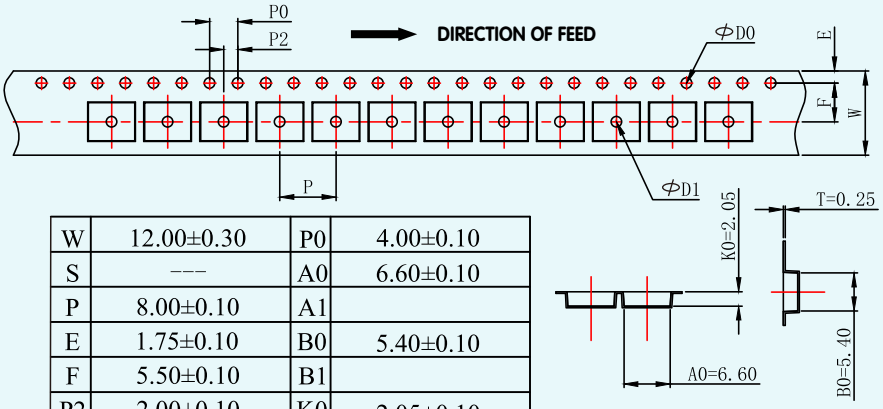
ESSOP10底面图

SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	-	-	1.50
A1	0.02	0.05	0.08
A2	1.30	1.40	1.50
A3	0.70	0.75	0.80
b	0.35	-	0.45
C	0.20	-	0.24
D	4.80	4.90	5.00
D1	3.30 REF		
e	1.00 BSC		
E	6.05	6.15	6.25
E1	3.82	3.92	4.02
E2	2.05 REF		
L	0.50	-	0.70
L1	1.15 REF		
H	0°	-	8°
h	0.30	0.40	0.50
g	0.05 REF		

TAPE AND REEL INFORMATION

REEL DIMENSIONS





W	12.00±0.30	P0	4.00±0.10
S	---	A0	6.60±0.10
P	8.00±0.10	A1	
E	1.75±0.10	B0	5.40±0.10
F	5.50±0.10	B1	
P2	2.00±0.10	K0	2.05±0.10
D0	1.50+0.10/-0.00	K1	
D1	1.50+0.10/-0.00	t	0.25±0.05

Precautions for MOS Circuit Operation:

Static electricity can be generated in many places. The following precautions can effectively prevent MOS circuit from being damaged due to the sound of electrostatic discharge:

- Operators shall be grounded through anti-static wrist strap.
- The equipment enclosure must be grounded.
- Tools used during assembly must be grounded.
- Conductor packaging or anti-static materials must be used for packaging or transportation.

Declaration:

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