OVERVOLTAGE AND OVERCURRENT PROTECTION IC AND Li+ CHARGER FRONT-END PROTECTION IC WITH LDO MODE

DESCRIPTION

The CS5805S is highly integrated circuits designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage,. The output acts as a linear regulator. The output is regulated to $V_{O(REG)}$ for inputs between $V_{O(REG)}$ and the overvoltage threshold. If an input overvoltage condition occurs, the IC immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. Additionally, the IC also monitors its own die temperature and switches off if it exceeds 140°C. The input overcurrent threshold is user-programmable.

FEATURES

- Provides Protection for Three Variables:
  -Input Overvoltage, with Rapid Response in < 1μs
  -User-Programmable Overcurrent with Current Limiting
- 30V pports up to 1.0A Input Current
- Robust Against False Triggering Due to Current Transients
- Thermal Shutdown
- Enable Input
- 5.45V LDO Mode Voltage Regulation

APPLICATIONS

- Mobile Phones and Smart Phones PDAs
- MP3 Players
- Low-Power Handheld Devices
- Bluetooth™ Headsets

Package

- SOT23_6L

TYPICAL APPLICATION CIRCUIT

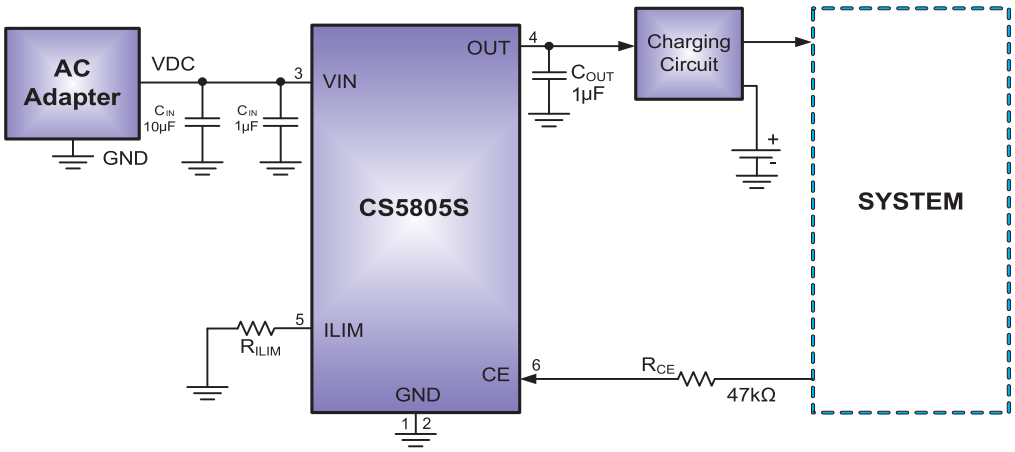
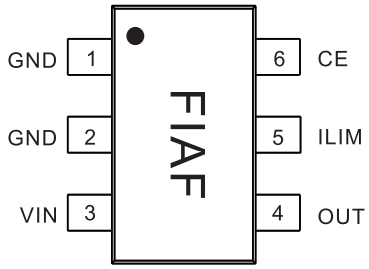


Figure a. Typical Application Circuit

PIN CONFIGURATION (TOP VIEW)

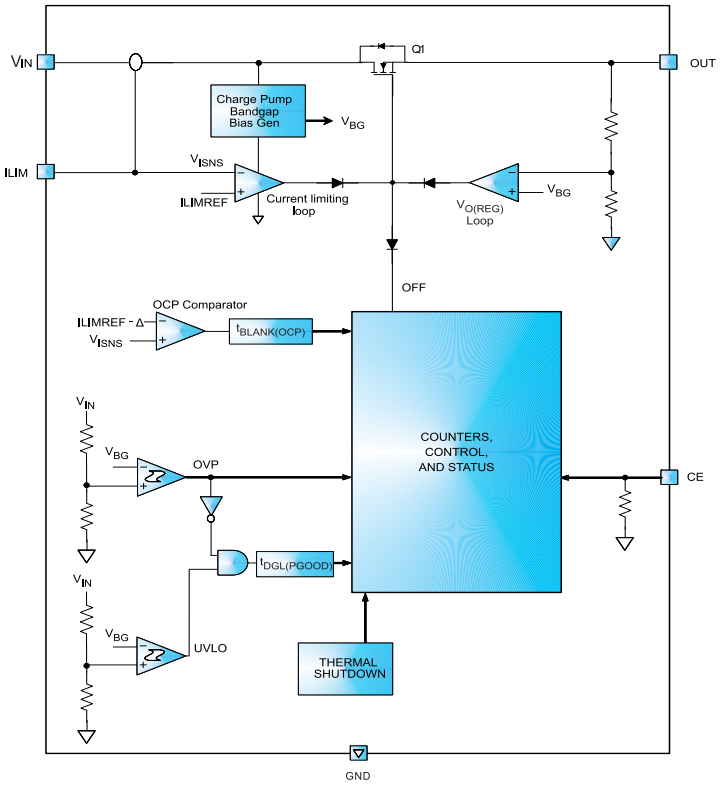


(SOT23-6)

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	PIN		
GND	1	–	Ground
GND	2	–	Ground
VIN	3	I	Input power. Connect IN to the external DC supply. Bypass IN to GND with a 1μF ceramic capacitor (minimum).
OUT	4	O	Output terminal to the charging system. Connect OUT to the external load circuitry. Bypass OUT to GND with a 1μF ceramic capacitor (minimum).
ILIM	5	I	Input overcurrent threshold programming. Connect a resistor from ILIM to GND to set the overcurrent threshold.
CE	6	I	Chip enable active low input. Connect CE = High to disable the IC and turn the input FET off. Connect CE = low for normal operation. CE is internally pulled down.

Simplified Block Diagram(Figure 1)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	PIN	VALUE	UNIT
V_I	Input voltage	IN (with respect to VSS)	–0.3 to 30	V
		OUT (with respect to VSS)	–0.3 to 7	
		ILIM, $\overline{CE}$,	–0.3 to 7	
I_I	Input current	IN	2	A
I_O	Output current	OUT	2	A
ESD	Withstand Voltage	All (Human Body)	2000	V
		All (Machine)	200	V
		All (Charge Device)	500	V
		IN (with IN bypassed to the VSS with a 1-μF low-ESR ceramic capacitor)	15 (Air Discharge) 8 (Contact)	kV
T_J	Junction temperature		–40 to 150	°C
T_{stg}	Storage temperature		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	3.3	30	V
I_{IN}	Input current, IN pin		1.2	A
I_{OUT}	Output current, OUT pin		1.2	A
$R_{(ILIM)}$	OCP Programming resistor	9	50	kΩ
T_J	Junction temperature	–40	125	°C

Order Information

Device	Package	Making	Reel Size	Tape Width	Quantity
CS5805S	SOT23-6L	FIAF XX	7"	8mm	**3000**

ELECTRICAL CHARACTERISTICS

over junction temperature range –40°C to 125°C and recommended supply voltage (unless otherwise noted)

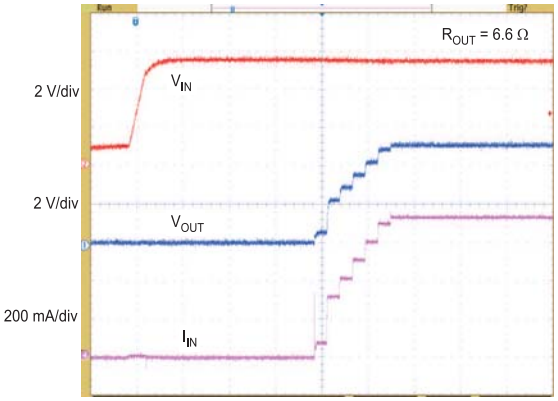
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN						
UVLO	Undervoltage lock-out, input power detected threshold	$\overline{CE}$ = Low, V_{IN} increasing from 0V to 3V	2.6	2.7	2.8	V
$V_{hys(UVLO)}$	Hysteresis on UVLO	$\overline{CE}$ = Low, V_{IN} decreasing from 3V to 0V	160	200	240	mV
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	$\overline{CE}$ = Low. Time measured from V_{IN} 0V → 5V 1μs rise-time, to output turning ON		16		ms
I_{DD}	Operating current	$\overline{CE}$ = Low, No load on OUT pin, V_{IN} = 5V, $R_{(ILIM)}$ = 25kΩ		580		μA
I_{STDBY}	Standby current	$\overline{CE}$ = High, V_{IN} = 5V		75	95	μA
INPUT TO OUTPUT CHARACTERISTICS						
V_{DO}	Drop-out voltage IN to OUT	$\overline{CE}$ = Low, V_{IN} = 5V, I_{OUT} = 1A		250	280	mV
$r_{DS(on)}$	Drain-sourceon-state resistance	$\overline{CE}$ = Low, V_{IN} = 5V, I_{OUT} = 1A		0.24		Ω
OUPUT VOLTAGE REGULATION						
$V_{O(REG)}$	Output voltage	$\overline{CE}$ = Low, V_{IN} = 5.7V, I_{OUT} = No Load		5.45	5.60	V
INPUT OVERVOLTAGE PROTECTION						
V_{OVP}	Input overvoltage protection threshold	$\overline{CE}$ = Low, V_{IN} increasing from 5V to 11V	5.85	6.1	6.4	V
$t_{PD(OVP)}$	Input OV propagation delay(1)	$\overline{CE}$ = Low		200		ns
$V_{hys(OVP)}$	Hysteresis on OVP	$\overline{CE}$ = Low, V_{IN} decreasing from 11V to 5V	20	100	110	mV
$t_{ON(OVP)}$	Recovery time from input overvoltage condition	$\overline{CE}$ = Low, Time measured from V_{IN} 7.5V → 5V, 1μs fall-time		16		ms
INPUT OVERCURRENT PROTECTION						
I_{OCP}	Input overcurrent protection threshold range		300		1000	mA
I_{OCP}	Input overcurrent protection threshold	$\overline{CE}$ = Low, $R_{(ILIM)}$ =15kΩ, 3 V ≤ V_{IN} < V_{OVP} – $V_{hys(OVP)}$	500	600	700	mA
$K_{(ILIM)}$	Adjustable current limit factor			9		A = kΩ
$t_{BLANK(OCP)}$	Blanking time, input overcurrent detected			240		μs
$t_{REC(OCP)}$	Recovery time from input overcurrent condition			128		ms
THERMAL PROTECTION						
$T_{J(OFF)}$	Thermal shutdown temperature			140	150	°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LEVELS ON $\overline{CE}$						
V_{IL}	Low-level input voltage		0		0.4	V
V_{IH}	High-level input voltage		1.4			V
I_{IL}	Low-level input current	$V_{(/CE)}$ = 0V			1	μA
I_{IH}	High-level input current	$V_{(/CE)}$ = 1.8V			15	μA

(1) Not tested in production. Specified by design.

TYPICAL PERFORMANCE CHARACTERISTICS

Test conditions (unless otherwise noted) for typical operating performance: V_{IN} = 5 V, C_{IN} = 1 µF, C_{OUT} = 1 µF, $R_{(ILIM)}$ = 25 kΩ, T_A = 25°C, V_{PU} = 3.3V

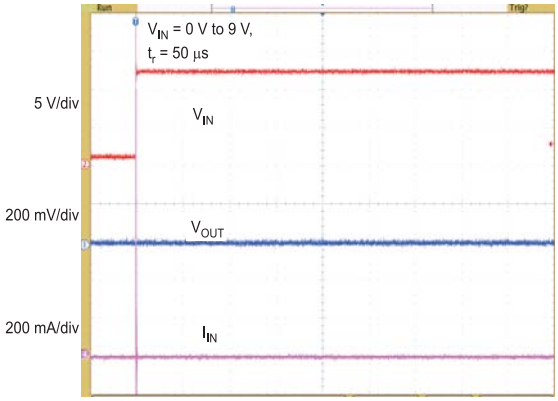
NORMAL POWER-ON SHOWING SOFT-START



t - Time - 2 ms/div

Figure 2.

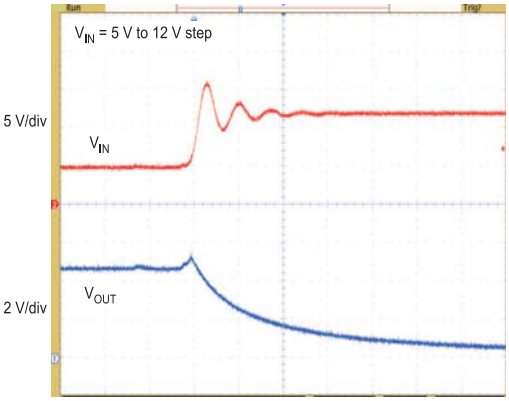
OVP AT POWER-ON



t - Time - 2 ms/div

Figure 3.

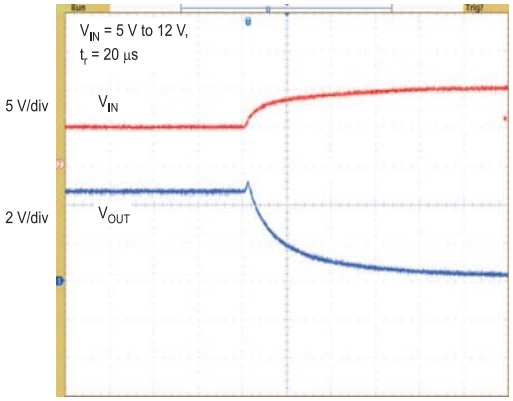
OVP RESPONSE FOR INPUT STEP



t - Time - 10 µs/div

Figure 4.

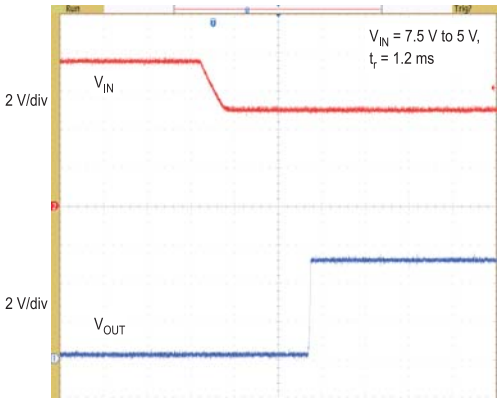
OVP RESPONSE FOR INPUT STEP



t - Time - 20 µs/div

Figure 5.

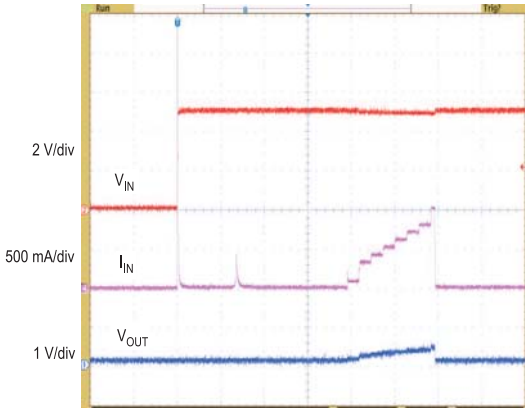
RECOVERY FROM OVP



t - Time - 4 ms/div

Figure 6.

OCP, ZOOM-IN ON THE FIRST CYCLE OF FIGURE 7



t - Time - 2 ms/div

Figure 7.

TYPICAL OPERATING PERFORMANCE (continued)

UNDERVOLTAGE LOCKOUT vs FREE-AIR TEMPERATURE

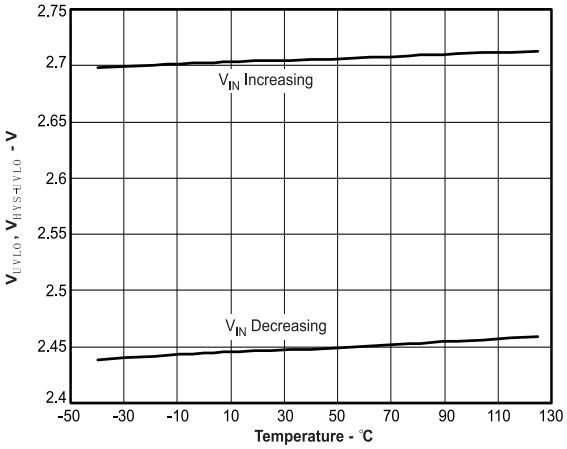


Figure 7

DROPOUT VOLTAGE (IN to OUT) vs FREE-AIR TEMPERATURE

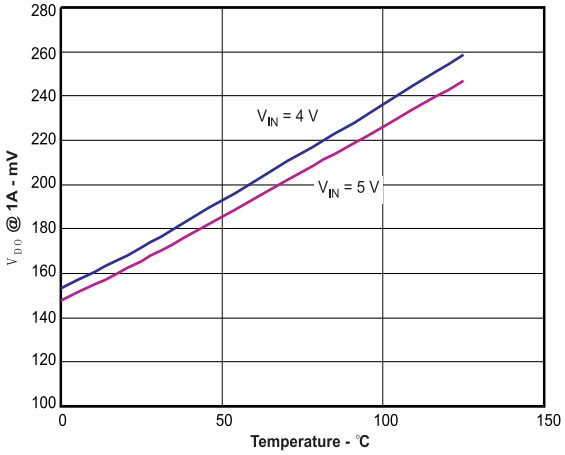


Figure 8

OVERVOLTAGE THRESHOLD PROTECTION vs FREE-AIR TEMPERATURE

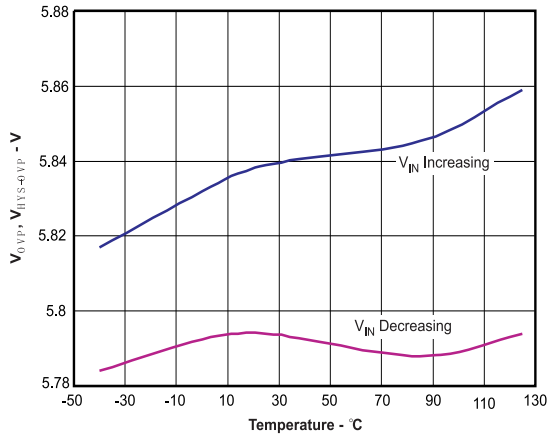


Figure 9

INPUT OVERCURRENT PROTECTION vs ILIM RESISTANCE

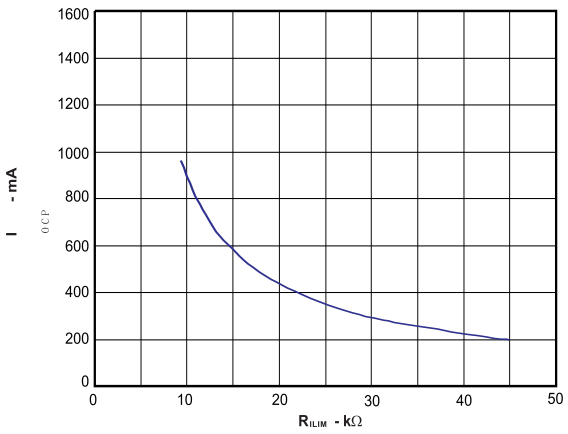


Figure 10.

INPUT OVERCURRENT PROTECTION vs FREE-AIR TEMPERATURE

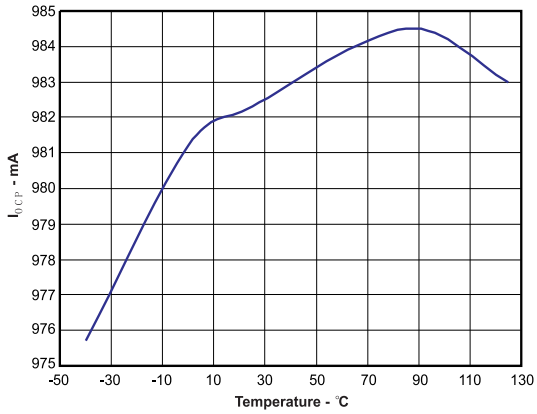


Figure 11.

SUPPLY CURRENT vs INPUT VOLTAGE

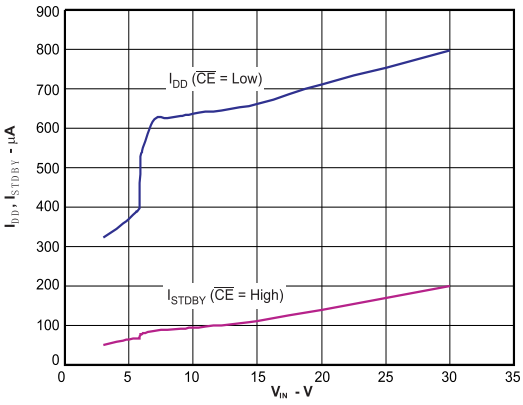
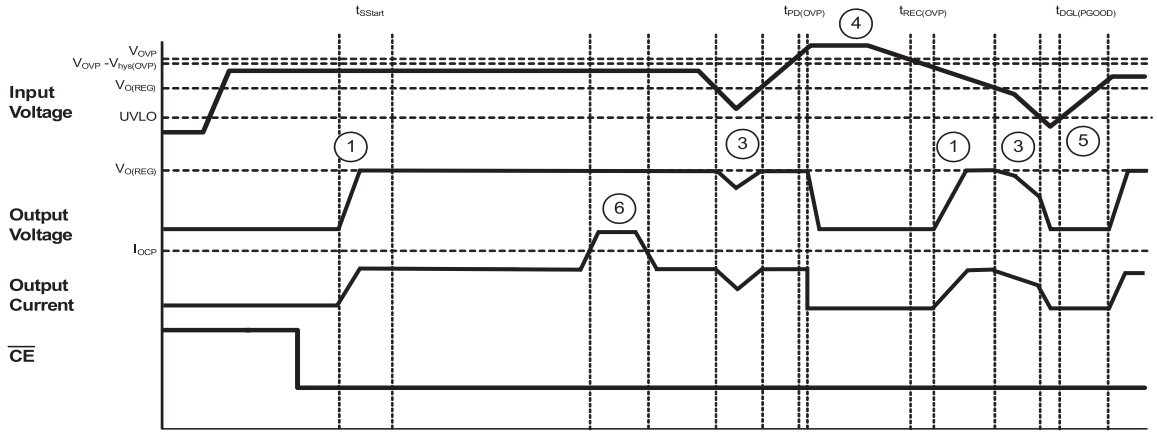


Figure12.

TIMING DIAGRAM



1. Normal start-up condition
2. $V_{UVLO} < V_{IN} < V_{O(REG)}$, V_{OUT} tracks V_{IN}
3. Input over-voltage event
4. Input below UVLO
5. High-current event during normal operation

DETAILED FUNCTIONAL DESCRIPTION

CS5805S is a integrated circuits designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage. For an input overvoltage condition, the IC immediately removes power from the charging circuit by turning off an internal switch. For an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. Additionally, the IC also monitors its own die temperature and switches off if it exceeds 140°C. The input overcurrent threshold is user-programmable. The IC can be controlled by a processor.

POWER DOWN

The device remains in power down mode when the input voltage at the IN pin is below the undervoltage threshold UVLO. The FET Q1 connected between IN and OUT pins is off.

POWER-ON RESET

The device resets when the input voltage at the IN pin exceeds the UVLO threshold. All internal counters and other circuit blocks are reset. The IC then waits for duration $t_{DGL(PGOOD)}$ for the input voltage to stabilize. FET Q1 is turned ON. The IC has a soft-start feature to control the inrush current. The soft-start minimizes the ringing at the input (the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit). Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, instead it will go into protection mode .

OPERATION

The device continuously monitors the input voltage, the input currentas described in detail in the following sections.

Input Overvoltage Protection

While the input voltage is less than $V_{O(REG)}$, the output voltage tracks the input voltage (less the drop due to the $R_{DS(on)}$ of Q1). When the input voltage is between $V_{O(REG)}$ and V_{OVP}, the device functions as a linear regulator and regulates the output voltage to 5.15V. If the input voltage rises above V_{OVP}, the internal FET Q1 is turned off, removing power to the output. The response is rapid, with the FET turning off in less than a microsecond.

Input Overcurrent Protection

The overcurrent threshold is programmed by a resistor $R_{(ILIM)}$ connected from the ILIM pin to VSS. Figure 10 shows the OCP threshold as a function of $R_{(ILIM)}$, and may be approximated by the following equation: $I_{OCP} = 9 \div R_{(ILIM)}$ (current in A, resistance in kΩ) If the load current tries to exceed the I_{OCP} threshold, the device limits the current for a blanking duration of $t_{BLANK(OCP)}$. If the load current returns to less than I_{OCP} before $t_{BLANK(OCP)}$ times out, the device continues to operate. However,if the overcurrent situation persists for $t_{BLANK(OCP)}$, the FET Q1 is turned off for a duration of $t_{REC(OCP)}$. The FET is then turned on again after $t_{REC(OCP)}$ and the current is monitored all over again.To prevent the input voltage from spiking up due to the inductance of the input cable, Q1 is turned off slowly, resulting in a “soft-stop”.

Thermal Protection

If the junction temperature of the device exceeds $T_{J(OFF)}$, the FET Q1 is turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

Enable Function

The IC has an enable pin which can be used to enable or disable the device. When the CE pin is driven high, the internal FET is turned off. When the CE pin is low, the FET is turned on if other conditions are safe. The CE pin has an internal pulldown resistor and can be left floating.

APPLICATION INFORMATION (WITH REFERENCE TO FIGURE a)

Selection of R_{CE}

The CE pin can be used to enable and disable the IC. If host control is not required, the CE pin can be tied to ground or left un-connected, permanently enabling the device.

In applications where external control is required, the CE pin can be controlled by a host processor. the CE pin should be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum V_{OH} of the host GPIO pin less the drop across the resistor should be greater than V_{IH} of the CS5805S CE pin. The drop across the resistor is given by $R_{CE} \times I_{IH}$.

Selection of Input and Output Bypass Capacitors

The input capacitor C_{IN} in Figure a is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from overshooting to dangerous levels. It is recommended that a ceramic capacitor of at least 1μF be used at the input of the device. It should be located in close proximity to the IN pin.C_{OUT} in Figure a is also important: If a fast (< 1μs rise time) overvoltage transient occurs at the input, the current that charges C_{OUT} causes the device's current-limiting loop to start, reducing the gate-drive to FET Q1. This results in improved performance for input overvoltage protection. C_{OUT} should also be a ceramic capacitor of at least 1μF, located close to the OUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

Powering Accessories

In some applications, the equipment that the protection IC resides in may be required to provide power to an accessory (e.g. a cellphone may power a headset or an external memory card) through the same connector pins that are used by the adapter for charging. Figure 13 and Figure 14 illustrate typical charging and accessory-powering scenarios:

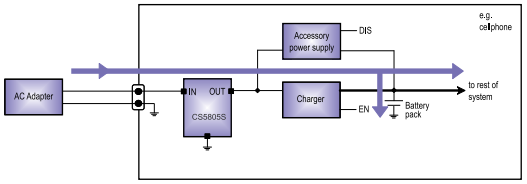


Figure 13 . Charging - The Red Arrows Show the Direction of Current Flow

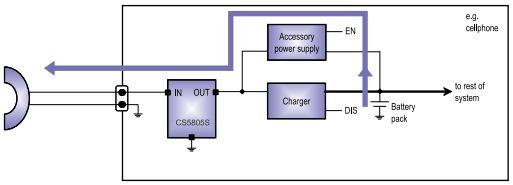
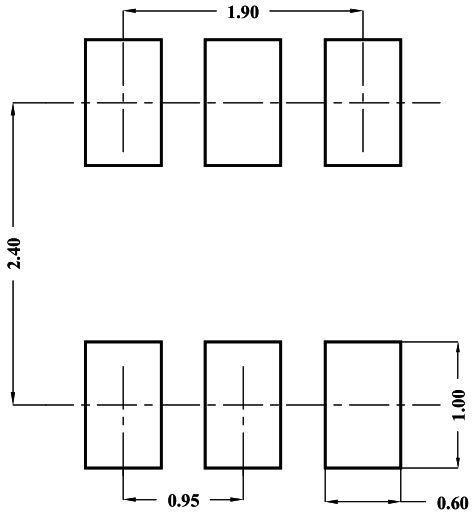


Figure 14 . Powering an Accessory - The Red Arrows Show the Direction of Current Flow

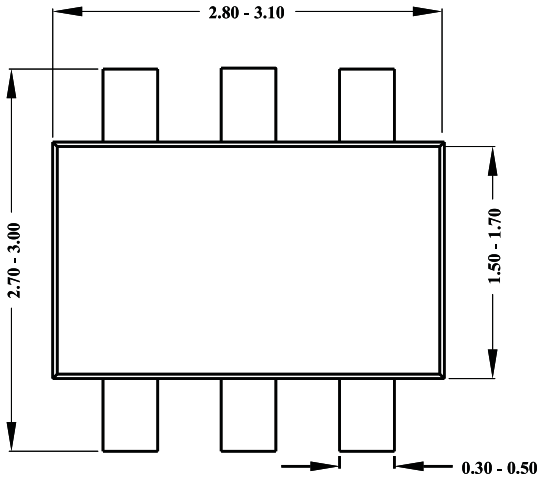
In the second case, when power is being delivered to an accessory, the CS5805S device is required to support current flow from the OUT pin to the IN pin. If V_{OUT} > UVLO + 0.7V, FET Q1 is turned on, and the reverse current does not flow through the diode but through Q1. Q1 remains ON as long as V_{OUT} > UVLO – $V_{hys(UVLO)}$ + $R_{DS(on)}$ × $I_{(ACCESSORY)}$. Within this voltage range, the reverse current capability is the same as the forward capability, 1.0A. It should be noted that there is no overcurrent protection in this direction.

PACKAGE INFORMATION

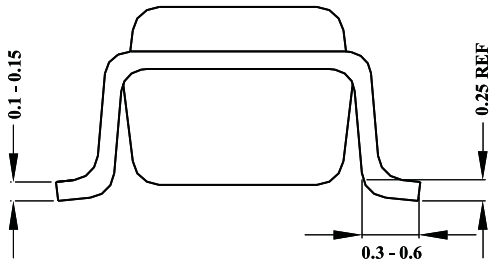
SOT23-6L Package Outline & PCB Layout

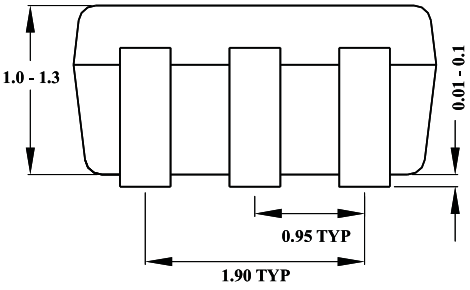


Recommended Pad Layout



Top View





Notes: **All dimension in MM**
All dimension don't not include mold flash & metal burr