

Built in Charge Pump Module, Fixed 28 Times Gain, AB/D switching, 3 Kinds of Anti Breaking Modes Are Optional, Peripheral Full Chip RC Application, 5.2W Mono Channel GF Class Audio Power Amplifier

General Description

CS5260E is a class GF single channel audio power amplifier with CMOS technology, which can provide up to 5.2W continuous power for 4Ω load; the internal fixed gain of chip effectively reduces the number of peripheral components; the application of peripheral full chip resistor and capacitor device can reduce the peripheral board area as much as possible, and reduce the cost increase caused by manual plug-in; It integrates two working modes of class D and class AB, which can not only ensure the strong power output in class D mode, but also eliminate the interference of power amplifier to the system in the case of FM; CS5260E has a unique anti breaking (NCN) function, which can automatically adjust the gain of power amplifier according to the size of the output signal, so as to achieve more comfortable auditory feeling.

In the mobile audio equipment powered by lithium battery, CS5260E is an ideal power amplifier solution for audio subsystem. The fully differential architecture and extremely high PSRR of CS5260E effectively improve the RF noise suppression ability of CS5260E. In addition, CS5260E has built-in over-current protection and overheating protection, which can effectively protect the chip from damage under abnormal working conditions. CS5260E offers the ESOP10 package type with a rated operating temperature range of -40°C to 85 °C.

Features

- Integrates Charge Pump Boost Module, Integration of Class AB and Class D Operation Modes, GF Class Audio Power Amplifier
- Output Power(Cout=1μF+22μF,NCN OFF@D MODE)
VBAT = 5.0V, THD+N=10% RL=4Ω@ 5.15W; RL=8Ω@ 3.0W;
VBAT = 5.0V, THD+N=1% RL=4Ω@ 4.2W; RL=8Ω@ 2.4W;
VBAT = 3.6V, THD+N=10% RL=4Ω@3.5W; RL=8Ω@ 2.8W;
VBAT = 3.6V, THD+N=1% RL=4Ω@2.95W; RL=8Ω@ 2.3W;
- Output Power(Cout=1μF+220μF,NCN OFF@D MODE)
VBAT = 5.0V, THD+N=10% RL=4Ω@5.2W; RL=8Ω@ 3.1W;
VBAT = 5.0V, THD+N=1% RL=4Ω@ 4.3W; RL=8Ω@ 2.4W;
VBAT = 3.6V, THD+N=10% RL=4Ω@4.0W; RL=8Ω@ 2.9W;
VBAT = 3.6V, THD+N=1% RL=4Ω@3.6W; RL=8Ω@ 2.4W;
- Input Voltage Range:2.7~5.5V
- Turn off current:<1μA
- Standby Current:20mA@5V
- Class D modulation frequency: 350KHz
- Anti Breaking Mode Switch
- AERC Patented Technology Provides Excellent Full Bandwidth EMI Suppression Capability
- Excellent "Pop Click" Noise Suppression
- High PSRR: - 80dB at 217Hz
- Over Temperature Protection
- Over Voltage Protection

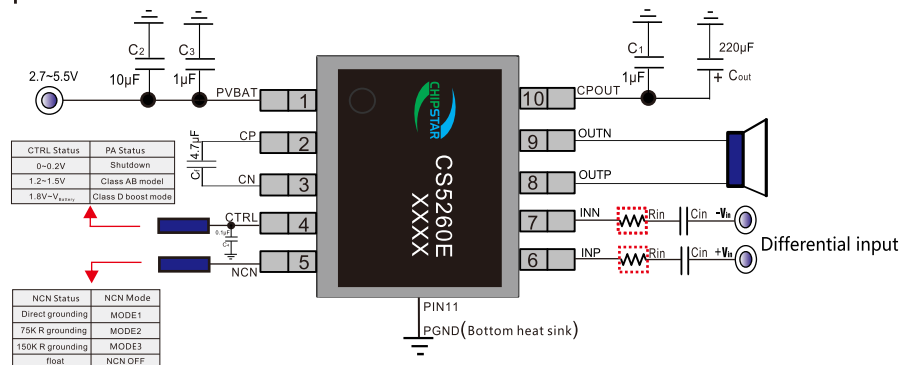
Applications

- Bluetooth Speaker
- Portable Audio Device

Package

- ESOP10L

Typical Applications

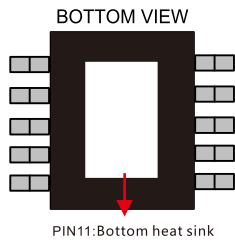
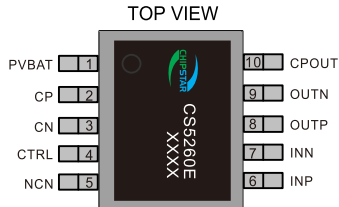


NOTES:

- (1) The heat sink at the bottom is the pin 11 (PGND) of CS5260E, which is connected to the earth.
- (2) In the figure, Rin in the red box is the reserved input resistance position, the CS5260E has 28 times of built-in gain, the internal integrated input resistance is 20K, and the feedback resistance is 560K, If gain is less than 28 times: Gain=560K/(20K+Rin)

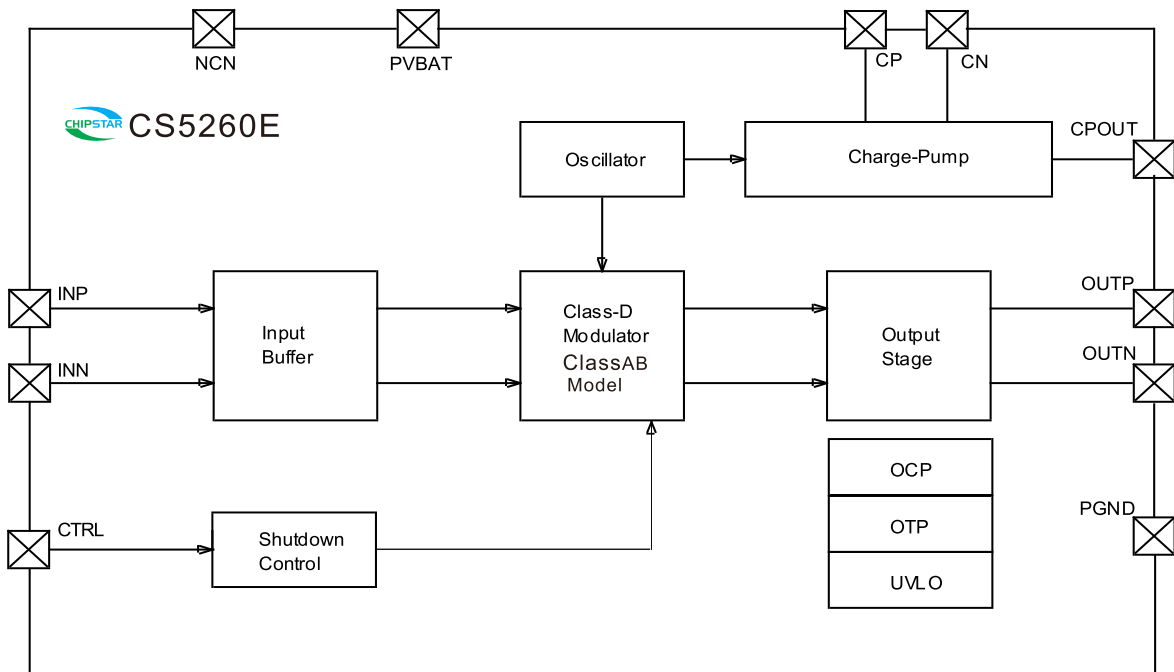
PIN Configuration and Functions

CS5260E(ESOP10 PACKAGE)



NO.	NAME	I/O	DESCRIPTION
1	PVBAT	P	Power supply pin, connected to external power supply
2	CP	I	Positive end of Flying capacitor
3	CN	I	Negative end of Flying capacitor
4	CTRL	I	Turn off / class AB class D switch control pin
5	NCN	I	Anti breaking mode control pin
6	INP	I	Audio input signal positive end
7	INN	I	Audio input signal Negative end
8	OUTP	O	Audio output signal positive end
9	OUTN	O	Audio output signal Negative end
10	CPOUT	P	Charge pump module power output pin
11	PGND (Bottom heat sink)	P	Power ground (bottom heat sink, connected to ground)

Functional Block Diagram



Absolute Maximum Ratings ¹

SYMBOL	PARAMETER	VALUE	UNIT
V _{DD}	Power supply without signal input	7.0	V
V _I	Input voltage	-0.3 to V _{DD} +0.3	V
T _J	Junction operating temperature range	-40 to 150	°C
T _{SDR}	Lead temperature (Soldering, 15 sec.)	220	°C
T _{STG}	Storage temperature range	-65 to 150	°C

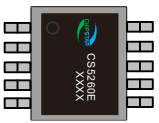
Recommended Operating Conditions

SYMBOL	PARAMETER	VALUE	UNIT
V _{DD}	Input voltage	2.7~5.5	V
T _A	Ambient temperature range	-40~85	°C
T _J	Junction operating temperature range	-40~150	°C

Thermal Information ²

SYMBOL	PARAMETER	VALUE	UNIT
θ _{JA} (ESOP10)	Package thermal resistance - chip to environment thermal resistance	45	°C/W
θ _{JC} (ESOP10)	Package thermal resistance - chip to package surface thermal resistance	10	°C/W

Ordering Information

Product Name	Package Type	Device Marking	Reel Size	Tape width	Quantity
CS5260E	ESOP10L		13"	12mm	4000
CS5260E	ESOP10L		Tube		100

ESD Range

HBM (Human Body Model) ----- ±4kV
 MM (Machine model) ----- ±400V

1. The above parameters are only the limit values of device operation. It is not recommended that the working conditions of the device exceed the limit values. Otherwise, the reliability and life of the device will be affected, and even permanent damage will be caused.

2. Where the PCB board is placed in CS5260E, a heat dissipation design is needed. The heat sink at the bottom of CS5260E is connected with the heat sink area of PCB board.

Electrical Characteristics ($T_A=25^{\circ}\text{C}$, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PVBAT	Supply voltage		2.7		5.5	V
$ V_{OS} $	Output offset voltage	VBAT=0V, $A_v=2\text{V/V}$ VBAT=3.0V to 5.0V		5	30	mV
PSRR	Power supply ripple rejection ratio	VBAT=2.7~5.5V, 217Hz		-80		dB
CMRR	Common mode rejection ratio	Input pin short circuit VBAT=2.7~5.5V		-72		dB
I_{DD}	Quiescent current	VBAT=3.7V, 无负载, 无滤波(D类)		20		mA
		VBAT=3.7V, 无负载(AB类)		10		
I_{SD}	Turn off current			0.1		μA
$r_{DS(ON)}$	Source drain on resistance (Mode D)	VBAT=3.7V		220		m Ω
		VBAT=5.0V		200		
Class D	modulation frequency	VBTA=2.7V to 5.5V		350		KHz
$f_{(SW:CH)}$	Charge Pump frequency	VBTA=2.7V to 5.5V		1700		KHz
R_{in}	Internal input resistance			20		K Ω
Over temperature protection	Temperature threshold			160		$^{\circ}\text{C}$
Over temperature exit	Temperature threshold			120		$^{\circ}\text{C}$
V_{CP}	Charge Pump output voltage	$I_{PDD}=100\text{mA}$	6.1	6.3	6.5	V
I_{CP}	Charge Pump output current	PVBAT=4.2V		1.8		A
T_{SS}	Charge Pump soft start time			500		μs
T_{st}	Chip start set time			120		ms
t_{MOD_D}	Setting time of D/AB mode conversion			120		ms

Working characteristics
 $T_A=25^{\circ}\text{C}$, Class D pattern, $C_f=4.7\mu\text{F}$, $f=1\text{KHz}$

SYMBOL	PARAMETER	TEST CONDITIONS	Cout=1 μF +22 μF		Cout=1 μF +220 μF		UNIT
			RL=4 Ω	RL=8 Ω	RL=4 Ω	RL=8 Ω	
P_O	output power	PVBAT=5.0V, THD=10%, NCN OFF	5.20	3.00	5.20	3.10	W
		PVBAT=5.0V, THD=1%, NCN OFF	4.20	2.40	4.20	2.40	
		PVBAT=4.2V, THD=10%, NCN OFF	4.60	2.90	4.90	3.00	
		PVBAT=4.2V, THD=1%, NCN OFF	3.80	2.30	4.10	2.40	
		PVBAT=3.6V, THD=10%, NCN OFF	3.50	2.80	4.00	2.90	
		PVBAT=3.6V, THD=1%, NCN OFF	2.95	2.30	3.60	2.40	
		PVBAT=3.4V, THD=10%, NCN OFF	3.00	2.40	3.60	2.40	
THD+N	Total harmonic distortion + noise	PVBAT=4.2V, $P_o=1.0\text{W}$, NCN OFF	0.10	0.08	0.10	0.10	%
		PVBAT=4.2V, $V_{pp}=300\text{mV}$, NCN OFF	0.15	0.20	0.20	0.15	
η	efficiency	PVBAT=4.2V, $P_o=0.5\text{W}$	78	82	80	83	%

 $T_A=25^{\circ}\text{C}$, RL=4 Ω Pure resistance, Class AB pattern, Cout=66 μF , $C_f=4.7\mu\text{F}$, $f=1\text{KHz}$, CTRL Voltage: 1.2~1.5V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	output power	PVBAT=4.0V, THD=10%		2.20		W
		PVBAT=4.0V, THD=1%		1.50		
		PVBAT=3.6V, THD=10%		1.70		
		PVBAT=3.6V, THD=1%		1.10		

T_A=25°C, Class D pattern, C_f=4.7μF, f=1KHz, NCN grounding

SYMBOL	PARAMETER	TEST CONDITIONS	C _{out} =1μF+22μF		C _{out} =1μF+220μF		UNIT
			RL=4Ω	RL=8Ω	RL=4Ω	RL=8Ω	
P _O	output power	PVBAT=5.0V, V _{pp} =300mV, NCN MODE1	4.30	2.40	4.40	2.40	W
		PVBAT=4.2V, V _{pp} =300mV, NCN MODE1	4.00	2.40	4.10	2.40	
		PVBAT=3.6V, V _{pp} =300mV, NCN MODE1	2.90	2.20	3.40	2.20	
THD+N	Total harmonic distortion + noise	PVBAT=4.2V, V _{pp} =300mV, NCN MODE1	1.70				%
		PVBAT=3.6V, V _{pp} =300mV, NCN MODE1	0.90				
T _{at}	Anti breaking start time		50				ms
T _{rl}	Anti breaking release time		300				ms

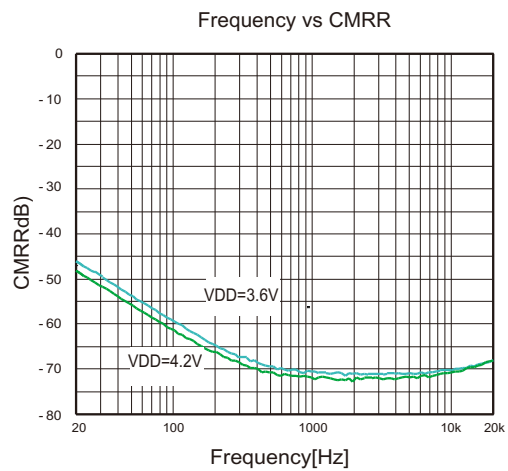
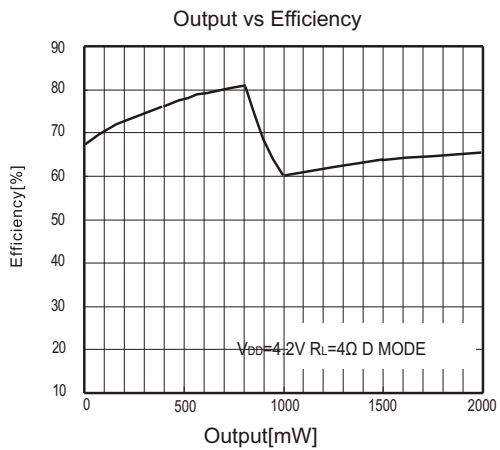
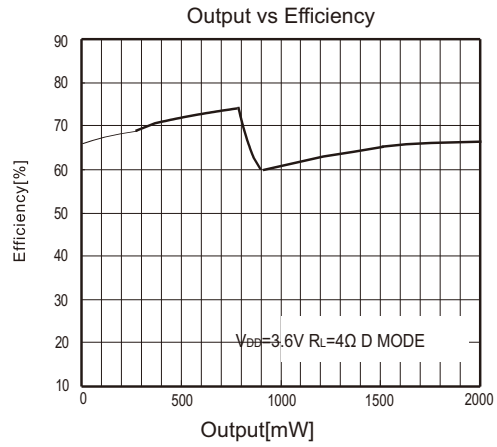
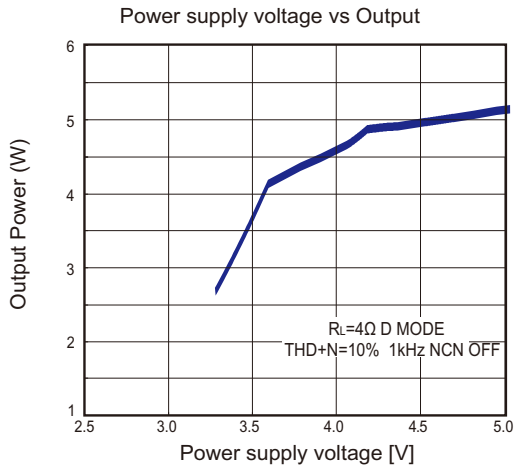
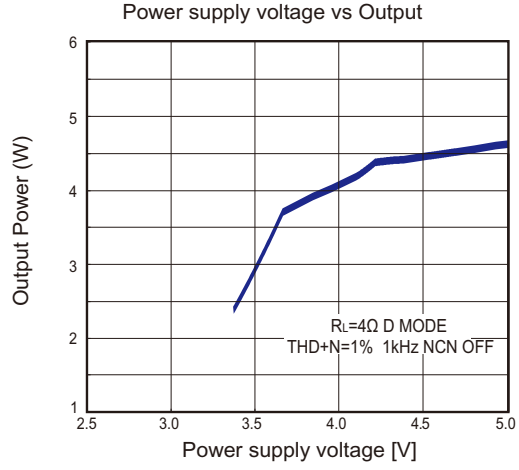
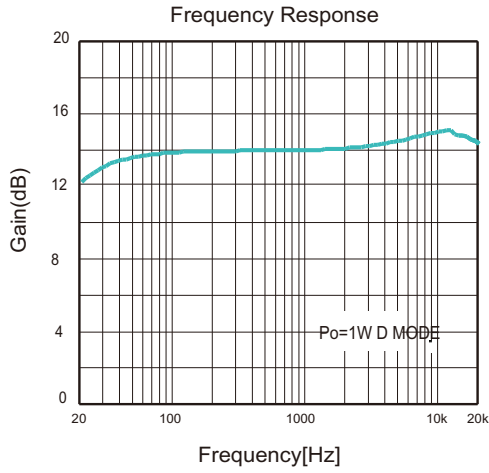
T_A=25°C, Class D pattern, C_f=4.7μF, f=1KHz, The NCN is grounded through a 75K Ω resistor

SYMBOL	PARAMETER	TEST CONDITIONS	C _{out} =1μF+22μF		C _{out} =1μF+220μF		UNIT
			RL=4Ω	RL=8Ω	RL=4Ω	RL=8Ω	
P _O	output power	PVBAT=5.0V, V _{pp} =300mV, NCN MODE2	3.30	2.00	3.30	2.00	W
		PVBAT=4.2V, V _{pp} =300mV, NCN MODE2	3.20	1.90	3.30	1.90	
		PVBAT=3.6V, V _{pp} =300mV, NCN MODE2	2.50	1.80	2.90	1.80	
THD+N	Total harmonic distortion + noise	PVBAT=4.2V, V _{pp} =300mV, NCN MODE2	0.50				%
		PVBAT=3.6V, V _{pp} =300mV, NCN MODE2	0.50				
T _{at}	Anti breaking start time		4				ms
T _{rl}	Anti breaking release time		2				s

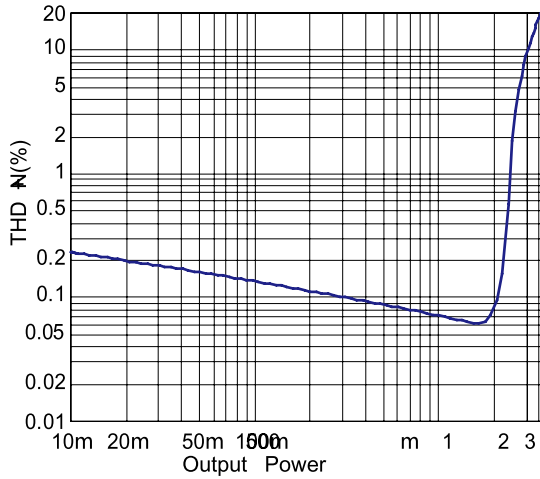
T_A=25°C, Class D pattern, C_f=4.7μF, f=1KHz, The NCN is grounded through a 150K Ω resistor

SYMBOL	PARAMETER	TEST CONDITIONS	C _{out} =1μF+22μF		C _{out} =1μF+220μF		UNIT
			RL=4Ω	RL=8Ω	RL=4Ω	RL=8Ω	
P _O	output power	PVBAT=5.0V, V _{pp} =300mV, NCN MODE3	4.80	2.70	4.90	2.80	W
		PVBAT=4.2V, V _{pp} =300mV, NCN MODE3	4.40	2.70	4.50	2.80	
		PVBAT=3.6V, V _{pp} =300mV, NCN MODE3	3.30	2.40	3.80	2.50	
THD+N	Total harmonic distortion + noise	PVBAT=4.2V, V _{pp} =300mV, NCN MODE3	6.50				%
		PVBAT=3.6V, V _{pp} =300mV, NCN MODE3	6.20				
T _{at}	Anti breaking start time		50				ms
T _{rl}	Anti breaking release time		75				ms

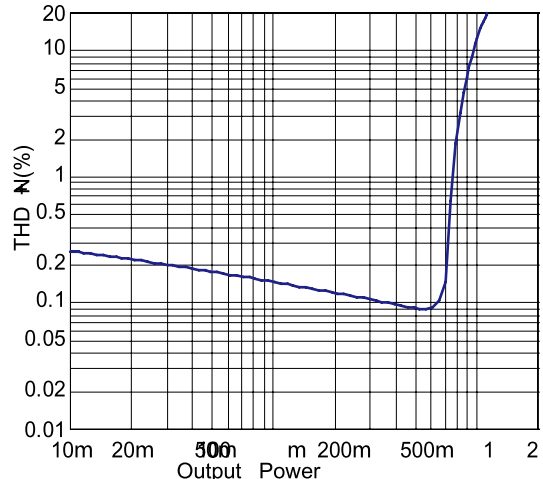
Typical Characteristics (TA=25°C, RL=4Ω, NCN OFF, D MODE)



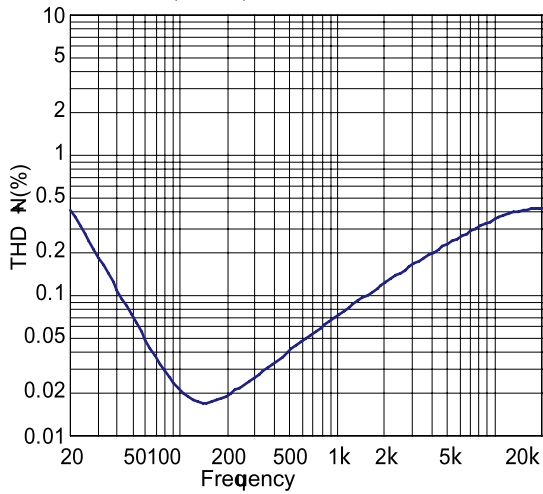
Typical Characteristics (TA=25°C, RL=4Ω, AB MODE, Charge Pump off)



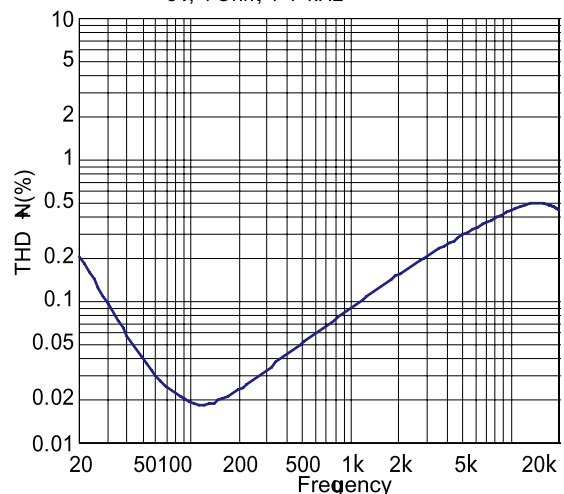
THD N vs Output Power
5V, 4 Ohm, f=1 kHz



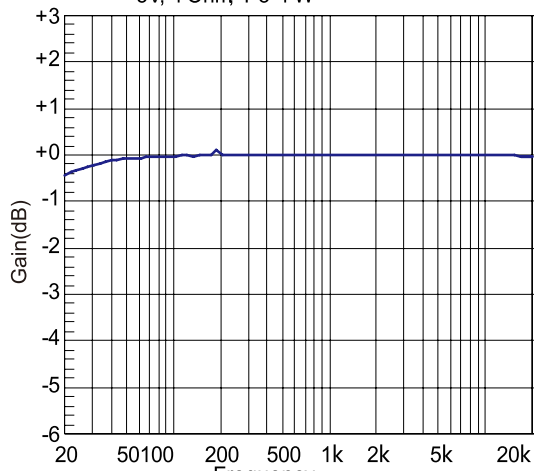
THD N vs Output Power
3V, 4 Ohm, f=1 kHz



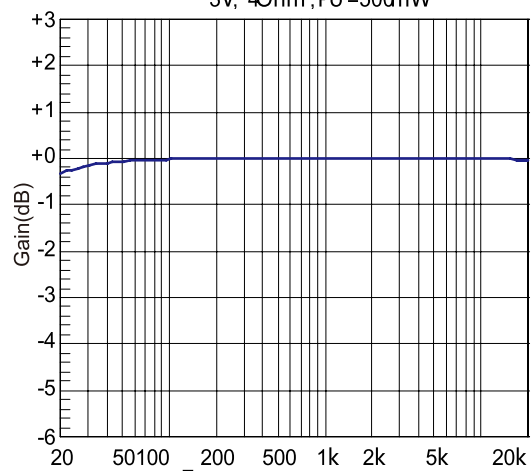
THD N vs Frequency
5V, 4 Ohm, Po=1W



THD N vs Frequency
3V, 4 Ohm, Po=500mW

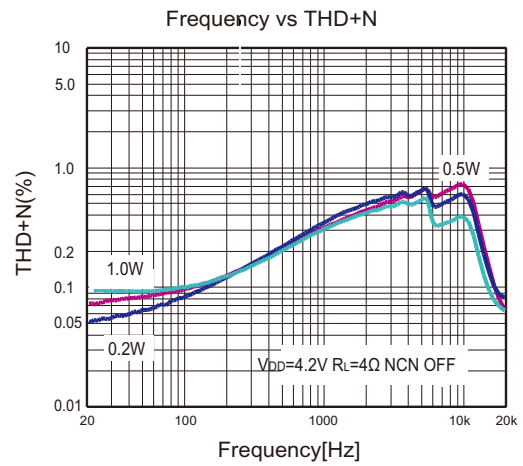
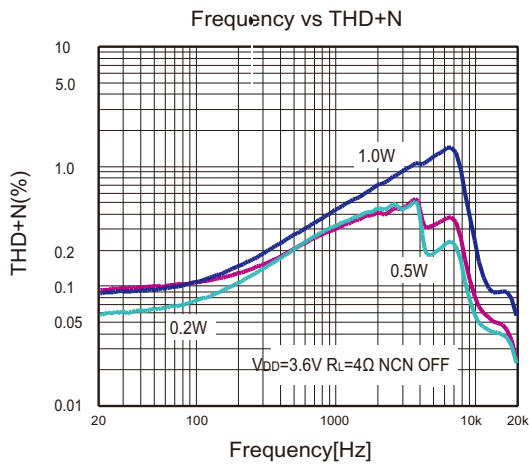
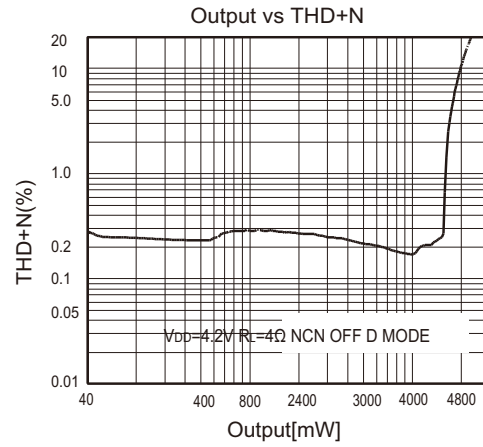
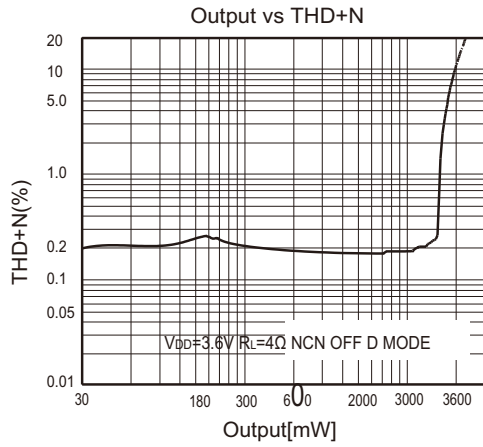


Frequency Response
5V, 4 Ohm



Frequency Response
3V, 4 Ohm

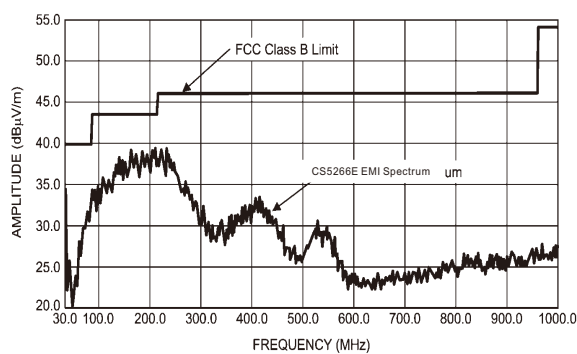
Typical Characteristics (TA=25°C, RL=4Ω, NCN OFF, D MODE)



Product Features

CS5260E has built-in charge pump boost module, which can be used for 4Ω. It provides up to 4.9W continuous power in the voltage range of lithium battery, and integrates class AB and class D audio amplifiers.

CS5260E adopts the proprietary AERC (adaptive edge rate control) technology, which greatly reduces the EMI interference in the full audio bandwidth. For the 60cm audio line, it has a margin of more than 20dB under the FCC standard (as shown in the figure below).



The PWM modulation structure without filter reduces the number of external components, PCB area and system cost, and simplifies the design. The chip has built-in overcurrent protection, overheat protection and undervoltage protection functions, which ensure that the chip is turned off under abnormal working conditions, effectively protecting the chip from damage. When the abnormal conditions are eliminated, CS5260E has the self recovery function to make the chip work again.

No Filter Required

CS5266E adopts PWM modulation without filter, which saves LC filter of traditional class D amplifier and improves efficiency. It provides a smaller area and lower cost implementation scheme for audio subsystem of portable devices.

Pop&Click Suppression

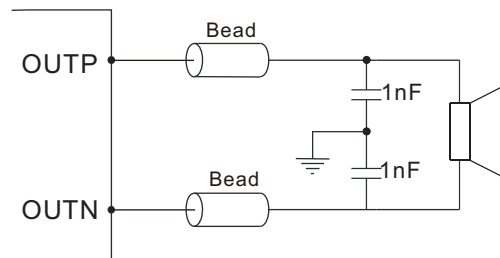
CS5266E has built-in special timing control circuit to achieve comprehensive pop&click suppression, which can effectively eliminate the transient noise that may appear when the system is powered on, down, wake up and shut down.

Protection Circuit

When the chip temperature is too high, the chip will be turned off. After the temperature drops, it can continue to work normally. When the power supply voltage is too low, the chip will also be turned off. After the power supply voltage is restored, the chip will start again.

Magnetic Beads and Capacitors

CS5260E can still meet the requirements of FCC standard for 60cm audio line without magnetic bead and capacitance. When the output audio line is too long or the device layout is close to EMI sensitive equipment, it is recommended to use magnetic beads and capacitors. Magnetic beads and capacitors should be placed as close to CS5260E as possible, as shown in the figure below.



Input Resistance (Rin)

The input of CS5260E is a differential amplifier structure, which can adopt single ended input connection method and differential input connection method. The setting of amplification factor of the two connection methods is the same. The CS5260E integrates 20KΩ Input resistance, feedback resistance is 560KΩ, Therefore, CS5260E has a fixed 28 times gain, and the amplification factor can be adjusted less than 28 times by changing the resistance of the external input resistor. The formula is as follows:

$$\text{Gain} = \frac{560\text{k}\Omega}{R_{in} + 20\text{k}\Omega} \left(\frac{V}{V} \right)$$

R_{in}: input resistance of external regulation

The good matching between the two input resistors is helpful to improve the performance of PSRR, CMRR and THD, so the resistor with accuracy of 1% is required. In PCB layout, the electronics should be placed close to CS5260E to prevent the introduction of noise from high resistance nodes.

Input Capacitance (Cin)

A high pass filter is formed between the input resistor and the input capacitor, and its cut-off frequency is as follows:

$$f_{c(-3\text{dB})} = \frac{1}{2\pi * (R_{in} + 20\text{K}) * C_{in}}$$

In the application, the smaller C_{in} capacitor is helpful to filter the 217Hz noise from the input, and the smaller capacitor is helpful to reduce the crackle and click when the power amplifier is turned on. Good matching between the two input capacitors is beneficial to improve the overall performance of the chip and suppress the crackle and click noise. It is recommended to use a capacitor with a tolerance of

Charge Pump Flying Capacitor (Cf)

Flying capacitor is used to transfer energy between power supply and charge pump load. The value of flying capacitor directly affects the load regulation rate and output driving ability of charge pump. If the flying capacitor is too small, it will affect the load adjustment rate and output driving ability of the charge pump, thus affecting the output power of the power amplifier. The larger the flying capacitor is, the stronger the load adjustment ability is, and the stronger the driving ability is. It is recommended to use X7R and X5R ceramic capacitors with voltage above 16V, 4.7uF and low ESR.

Charge Pump Holding Capacity (Cout)

The holding capacitance and ESR of the charge pump directly affect the ripple of the output voltage of the charge pump, thus affecting the performance of the power amplifier. Recommended 66μF Above, low ESR electrolytic capacitor. As the output voltage of the charge pump is 6.3V, the holding capacitor needs to be 10V.

Power supply decoupling capacitor (Cs)

Good decoupling capacitor can improve the efficiency and performance of power amplifier. It is recommended to use X7R or X5R ceramic capacitor with low ESR. In the application of CS5260E, Pin1 is the power supply pin, which mainly provides current for the internal charge pump circuit. This capacitor is similar to the charge reservoir, which can provide current faster than the battery, so it helps to stabilize the power supply voltage and prevent the rapid fluctuation of voltage. It is recommended to place a 1uF and a 10uF low ESR capacitor as close as possible to Pin1 pin.

CTRL Pin Setting

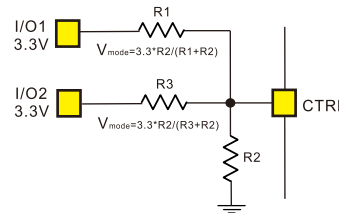
By setting the input level of the CTRL pin, you can enter various working modes of CS5260E, as shown in the table below:

CTRL Status	PA Status
0~0.2V	Shutdown
1.2~1.5V	Class AB model
1.8V~V _{Battery}	Class D boost mode

Based on the control mode in the above table, the following settings can be made according to the system in actual use:

If the main control IO control voltage is 3.3V, as shown in the figure, with the help of two IO ports and voltage divider line to realize the switching of various working states. When IO1 and IO2 are at low level, CS5260E enters shutdown mode; When IO1 is high and IO2 is suspended, CS5260E will enter class AB mode if Vctrl voltage is between 1.2 V and 1.5V by selecting appropriate resistance ratio of R1 and R2; When IO1 is

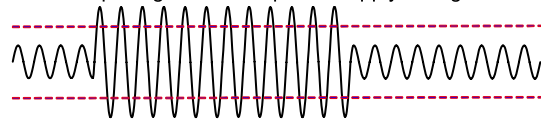
suspended and IO2 is at high level, CS5260E enters class D boost mode as long as appropriate R3 and R2 resistance ratio are selected to make Vctrl voltage greater than 1.8V; The absolute values of R1, R2 and R3 are determined by the acceptable power consumption, and the CTRL does not need the driving current.



NCN function

In audio applications, the input signal is too large or the battery voltage drops and other factors will lead to the output signal of audio power amplifier broken sound distortion, and the overload signal will cause permanent damage to the speaker. CS5260E's unique NCN function can detect the distortion of the amplifier's output signal and automatically adjust the system gain to keep the output audio signal smooth. It not only effectively avoids the damage of high-power overload output to the speaker, but also brings more comfortable hearing enjoyment.

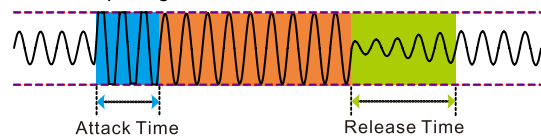
Audio output signal without power supply voltage limitation



Audio output signal in NCNOFF mode



Audio output signal in NCN mode



NCN Function Diagram

PCB design considerations

In order to give full play to the performance of CS5260E, the layout and wiring of PCB must be carefully considered

1: Try to walk a short and thick power line to CS5260E alone. It is recommended that the width of copper wire is greater than 1 mm. The decoupling capacitor should be placed as close to the power supply pin as possible.

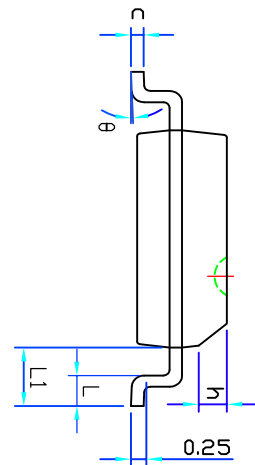
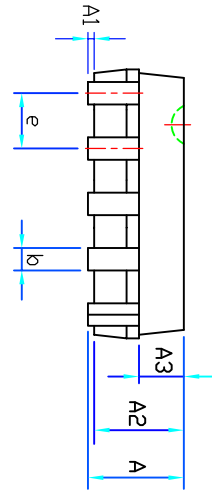
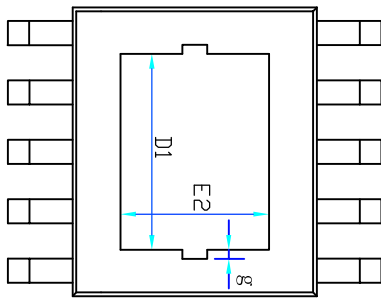
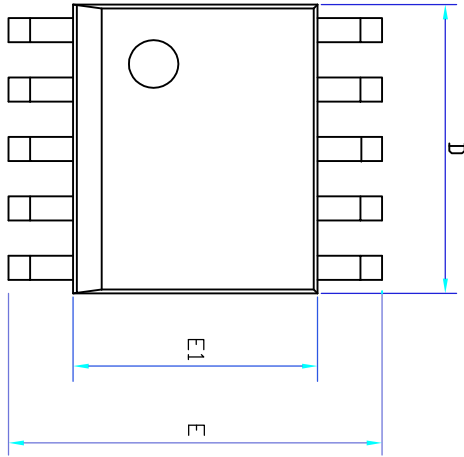
2: The flying capacitor should be placed close to CN and CP pins of CS5260E as far as possible, the output capacitor Cout should be placed close to CPOUT pin, and the connection between capacitor and chip pin should be as short and thick as possible.

3: The input capacitance and resistance of CS5260E should be placed as close as possible to the INN and INP pins of the chip, and the input lines should be parallel to suppress noise coupling.

4: The magnetic beads and capacitors should be placed close to the OUTN and OUTP pins of the chip. The output line from the chip to the horn should be as short and thick as possible. The recommended copper wire width is 0.5mm.

5: In order to obtain good heat dissipation performance, the heat sink and GND pin of CS5260E should be directly connected to the large area of the layer, and the heat sink should be connected to the middle layer through the through hole.

Package Information: CS5260E ESOP10L



SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	—	—	1.50
A1	0.02	0.05	0.08
A2	1.30	1.40	1.50
A3	0.70	0.75	0.80
b	0.35	—	0.45
c	0.20	—	0.24
D	4.80	4.90	5.00
D1	3.10REF		
e	1.00BSC		
E	6.05	6.15	6.25
E1	3.82	3.92	4.02
E2	2.20REF		
L	0.50	—	0.70
L1	1.15REF		
h	0.30	0.40	0.50
θ	0	—	8°
g	0.15REF		