

Built in Charge Pump Module, Fixed 28 Times Gain, AB/D switching, 2 Kinds of Anti Breaking Modes Are Optional, Peripheral Full Chip RC Application, 5.2W Mono Channel GF Class Audio Power Amplifier

General Description

CS5230E is a class GF single channel audio power amplifier with CMOS technology, which can provide up to 5.2W continuous power for 4Ω load; the internal fixed gain of chip effectively reduces the number of peripheral components; the application of peripheral full chip resistor and capacitor device can reduce the peripheral board area as much as possible; It integrates two working modes of class D and class AB, which can not only ensure the strong power output in class D mode, but also eliminate the interference of power amplifier to the system in the case of FM; CS5230E has a unique anti breaking (NCN) function, which can automatically adjust the gain of power amplifier according to the size of the output signal, so as to achieve more comfortable auditory feeling. It also has power self-adaptive capability. When the power supply voltage is low, the power amplifier will automatically reduce the gain, so as to reduce the output power of the power amplifier. The periphery of CS5230E only has low-cost resistance capacitance devices. In the mobile audio equipment powered by lithium battery, CS5230E is an ideal power amplifier solution for audio subsystem. The fully differential architecture and extremely high PSRR of CS5230E effectively improve the RF noise suppression ability of CS5230E. In addition, CS5230E has built-in over-current protection, short circuit protection and overheating protection, which can effectively protect the chip from damage under abnormal working conditions. CS5260E offers the ESOP10 package type with a rated operating temperature range of -40°C to 85 °C.

Features

- Integrates Charge Pump Boost Module, Integration of Class AB and Class D Operation Modes, GF Class Audio Power Amplifier
- Advanced power adaptation
- Output Power
 - Po at VBAT = 5.0V, RL=4Ω+33uH
 - THD+N=10% 5.2W(NCN OFF@D MODE)
 - THD+N=1% 4.3W(NCN OFF@D MODE)
 - Po at VBAT = 4.2V, RL=4Ω+33uH
 - THD+N=10% 4.8W(NCN OFF@D MODE)
 - THD+N=1% 4.1W(NCN OFF@D MODE)
 - Po at VBAT = 3.6V, RL=4Ω+33uH
 - THD+N=10% 3.45W(NCN OFF@D MODE)
 - THD+N=1% 3.00W(NCN OFF@D MODE)
- Input Voltage Range: 2.7~5.5V
- Turn off current: <1μA
- Standby Current: 3mA
- Class D modulation frequency: 300KHz
- Anti Breaking Mode Switch
- AERC Patented Technology Provides Excellent Full Bandwidth EMI Suppression Capability
- Excellent "Pop Click" Noise Suppression
- High PSRR: - 80dB at 217Hz
- Over Temperature Protection
- Over Voltage Protection

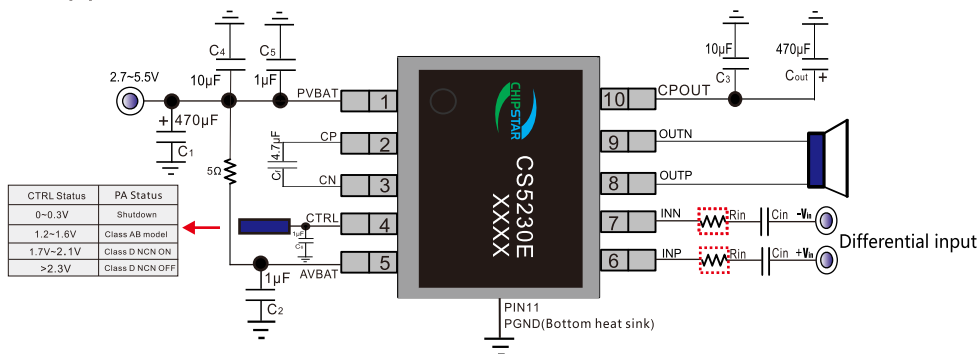
Applications

- Bluetooth Speaker
- Portable Audio Device

Package

- ESOP10L

Typical Applications

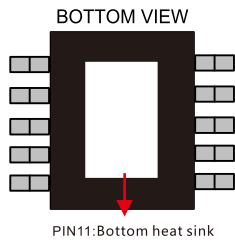
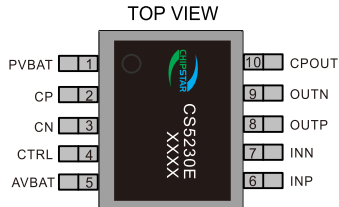


NOTES:

- (1) C₁ (Flyin capacitor) requires a chip capacitor with a withstand voltage of more than 16V X5R
- (2) The heat sink at the bottom is the pin 11 (PGND) of CS5230E, which is connected to the earth.
- (3) In the figure, Rin in the red box is the reserved input resistance position, the CS5230E has 28 times of built-in gain, the internal integrated input resistance is 20K, and the feedback resistance is 560K, If gain is less than 28 times: Gain=560K/(20K+Rin)

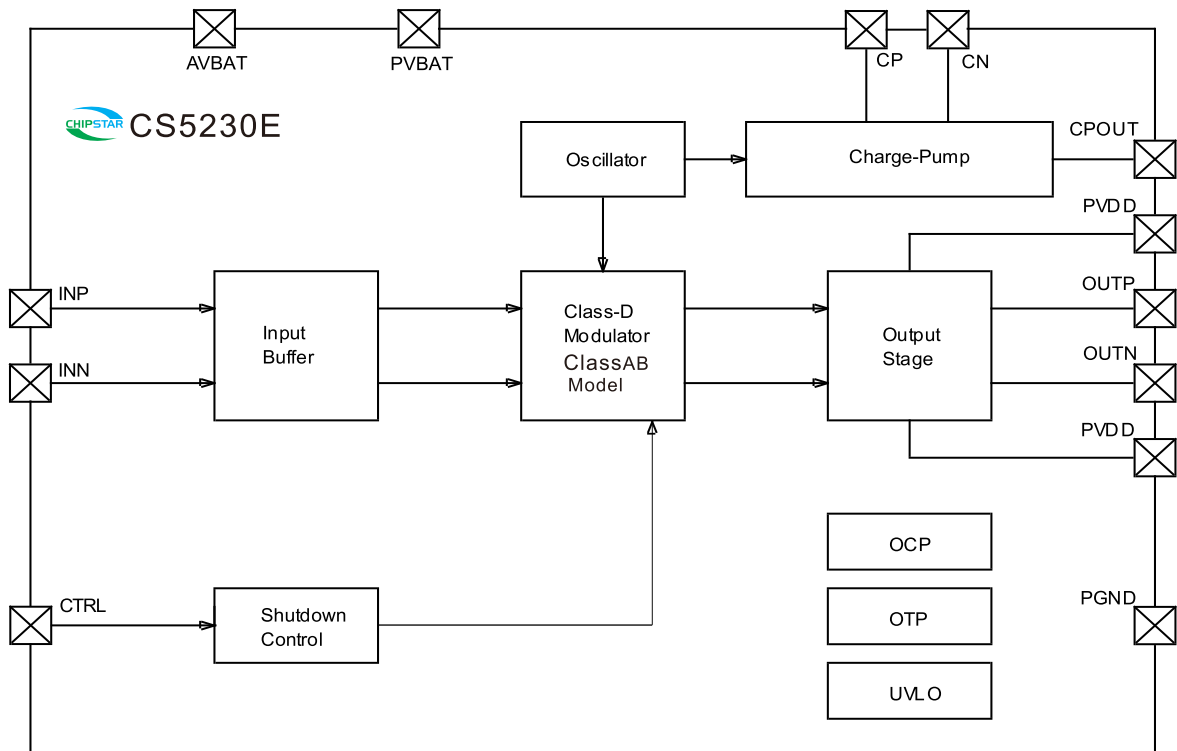
PIN Configuration and Functions

CS5230E(ESOP10 PACKAGE)



NO.	NAME	I/O	DESCRIPTION
1	PVBAT	P	Power supply pin, connected to external power supply
2	CP	I	Positive end of Flying capacitor
3	CN	I	Negative end of Flying capacitor
4	CTRL	I	Turn off / class AB class D switch control pin
5	AVBAT	I	Analog power supply, connected to external power supply
6	INP	I	Audio input signal positive end
7	INN	I	Audio input signal Negative end
8	OUTP	O	Audio output signal positive end
9	OUTN	O	Audio output signal Negative end
10	CPOUT	P	Charge pump module power output pin
11	PGND (Bottom heat sink)	P	Power ground (bottom heat sink, connected to ground)

Functional Block Diagram



Absolute Maximum Ratings ¹

SYMBOL	PARAMETER	VALUE	UNIT
V _{DD}	Power supply without signal input	7.0	V
V _I	Input voltage	-0.3 to V _{DD} +0.3	V
T _J	Junction operating temperature range	-40 to 150	°C
T _{SDR}	Lead temperature (Soldering, 15 sec.)	220	°C
T _{STG}	Storage temperature range	-65 to 150	°C

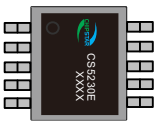
Recommended Operating Conditions

SYMBOL	PARAMETER	VALUE	UNIT
V _{DD}	Input voltage	2.7~5.5	V
T _A	Ambient temperature range	-40~85	°C
T _J	Junction operating temperature range	-40~150	°C

Thermal Information ²

SYMBOL	PARAMETER	VALUE	UNIT
θ _{JA} (ESOP10)	Package thermal resistance - chip to environment thermal resistance	45	°C/W
θ _{Jc} (ESOP10)	Package thermal resistance - chip to package surface thermal resistance	10	°C/W

Ordering Information

Product Name	Package Type	Device Marking	Reel Size	Tape width	Quantity
CS5230E	ESOP10L		13"	12mm	4000
CS5230E	ESOP10L		Tube		50

ESD Range

HBM (Human Body Model) ----- ±4kV
 MM (Machine model) ----- ±400V

1. The above parameters are only the limit values of device operation. It is not recommended that the working conditions of the device exceed the limit values. Otherwise, the reliability and life of the device will be affected, and even permanent damage will be caused.

2. Where the PCB board is placed in CS5230E, a heat dissipation design is needed. The heat sink at the bottom of CS5230E is connected with the heat sink area of PCB board.

Electrical Characteristics ($T_A=25^{\circ}\text{C}$, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PVBAT	Supply voltage		2.7		5.5	V
$ V_{OS} $	Output offset voltage	VBAT=0V, $A_v=2\text{V/V}$ VBAT=3.0V to 5.0V		5	30	mV
PSRR	Power supply ripple rejection ratio	VBAT=2.7~5.5V, 217Hz		-80		dB
CMRR	Common mode rejection ratio	Input pin short circuit VBAT=2.7~5.5V		-72		dB
I_{DD}	Quiescent current	VBAT=3.7V, No load, NO filtering (Class D)		3		mA
		VBAT=3.7V, No load, (Class AB)		10		
I_{SD}	Turn off current			0.1		μA
$r_{DS(ON)}$	Source drain on resistance (Mode D)	VBAT=3.7V		220		m Ω
		VBAT=5.0V		200		
$f_{(SW:D)}$	Class D modulation frequency	VBTA=2.7V to 5.5V		300		KHz
$f_{(SW:CH)}$	Charge Pump modulation frequency	VBTA=2.7V to 5.5V		1600		KHz
R_{in}	Internal input resistance			20		K Ω
T_{SD}	Over temperature protection temperature threshold			160		$^{\circ}\text{C}$
T_{SDR}	Over temperature exit temperature threshold			120		$^{\circ}\text{C}$
V_{CPOUT}	Charge Pump output voltage	$I_{PVDD}=100\text{mA}$	6.0	6.2	6.4	V
I_{CPOUT}	Charge Pump Maximum output current	PVBAT=4.2V		1.8		A
T_{SS}	Charge Pump soft start time			500		μs
T_{st}	Chip start set time			120		ms
t_{MOD_D}	Setting time of D/AB mode conversion			120		ms

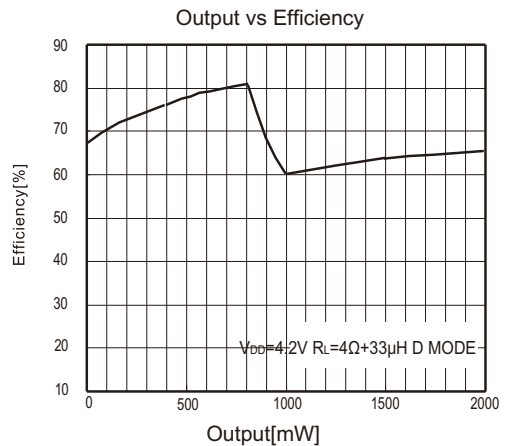
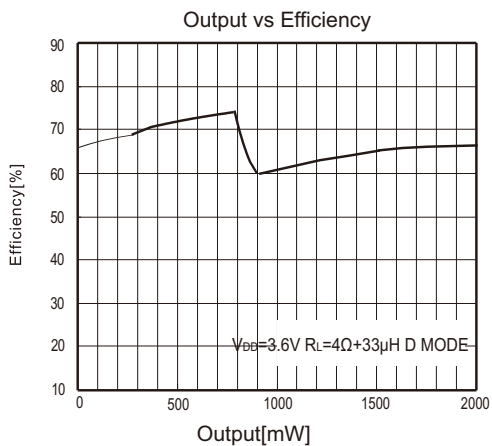
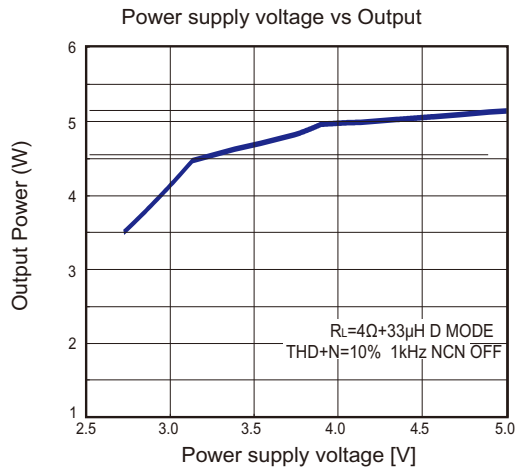
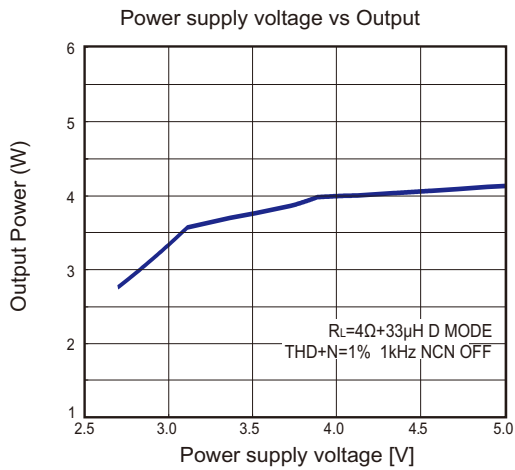
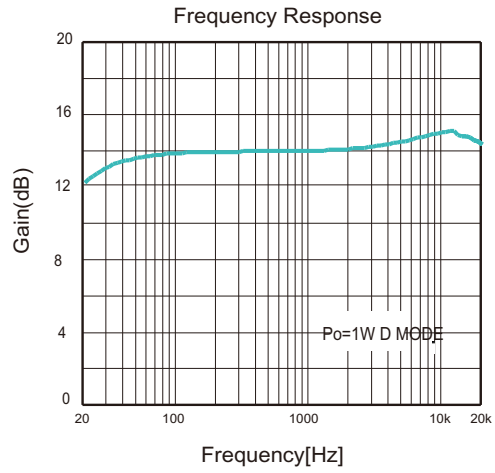
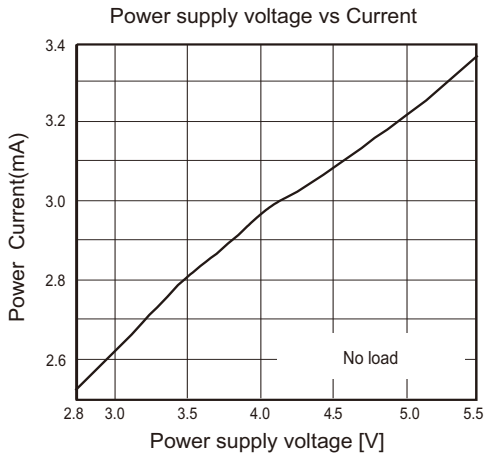
Working characteristics
 $T_A=25^{\circ}\text{C}$, $R_L=4\Omega+33\mu\text{H}$, Class D pattern, $C_{out}=470\mu\text{F}$, $C_f=4.7\mu\text{F}$, $f=1\text{KHz}$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	output power	PVBAT=5.0V, THD=10%, $V_{ctrl}>2.3\text{V}$, NCN OFF		5.30		W
		PVBAT=5.0V, THD=1%, $V_{ctrl}>2.3\text{V}$, NCN OFF		4.30		
		PVBAT=4.2V, THD=10%, $V_{ctrl}>2.3\text{V}$, NCN OFF		4.80		
		PVBAT=4.2V, THD=1%, $V_{ctrl}>2.3\text{V}$, NCN OFF		4.10		
		PVBAT=3.6V, THD=10%, $V_{ctrl}>2.3\text{V}$, NCN OFF		3.45		W
		PVBAT=3.6V, THD=1%, $V_{ctrl}>2.3\text{V}$, NCN OFF		3.00		
		PVBAT=5.0V, $V_{pp}=300\text{mV}$, $1.7\text{V}>V_{ctrl}>2.2\text{V}$		3.90		
		PVBAT=4.2V, $V_{pp}=300\text{mV}$, $1.7\text{V}>V_{ctrl}>2.2\text{V}$		3.60		
THD+N	Total harmonic distortion + noise	PVBAT=4.2V, $P_o=1.0\text{W}$, $V_{ctrl}>2.3\text{V}$, NCN OFF		0.05		%
		PVBAT=4.2V, $V_{pp}=300\text{mV}$, $1.7\text{V}>V_{ctrl}>2.2\text{V}$		0.27		
η	efficiency	PVBAT=4.2V, $P_o=0.5\text{W}$		82		%
T_{at}	Anti breaking start time	$V_{pp}=300\text{mV}$, $1.7\text{V}>V_{ctrl}>2.2\text{V}$		50		ms
T_{rl}	Anti breaking release time	$V_{pp}=300\text{mV}$, $1.7\text{V}>V_{ctrl}>2.2\text{V}$		75		ms

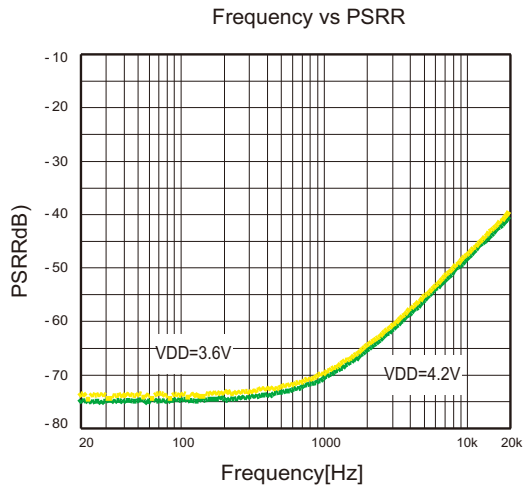
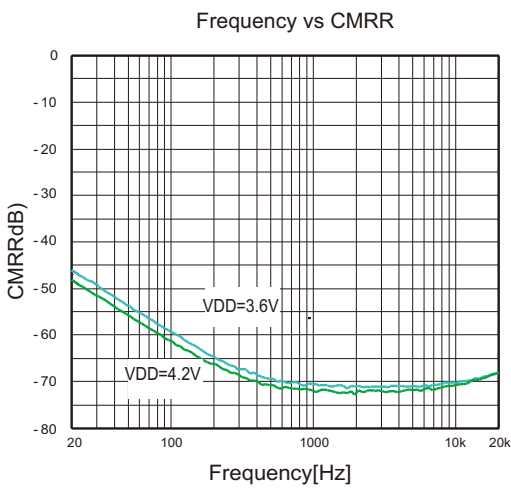
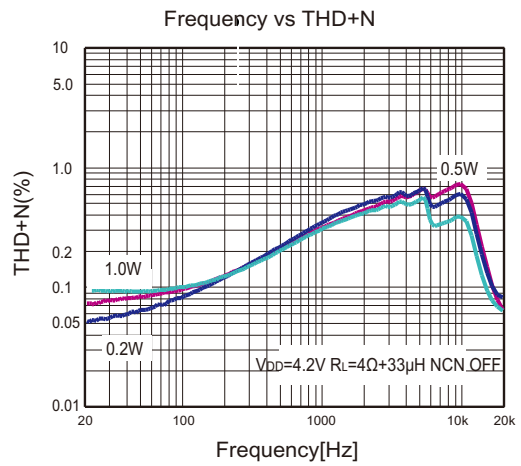
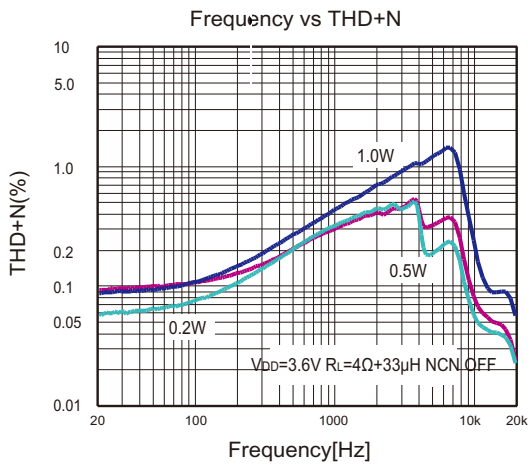
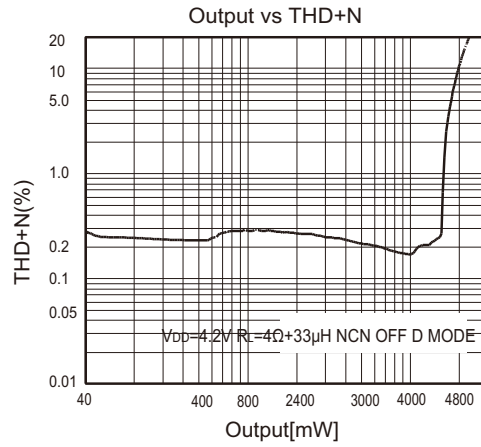
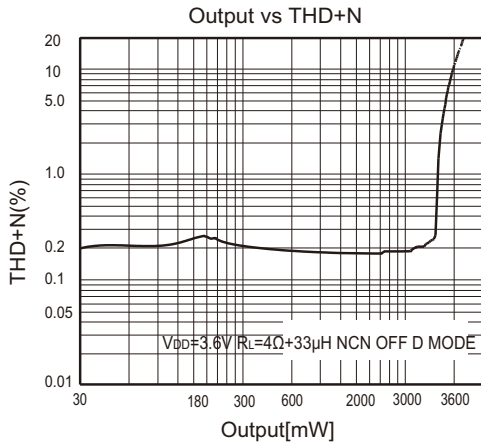
 $T_A=25^{\circ}\text{C}$, $R_L=4\Omega$ Pure resistance, Class AB pattern, $C_{out}=470\mu\text{F}$, $C_f=4.7\mu\text{F}$, $f=1\text{KHz}$, CTRL Voltage: 1.2~1.5V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	output power	PVBAT=4.0V, THD=10%		2.20		W
		PVBAT=4.0V, THD=1%		1.50		
		PVBAT=3.6V, THD=10%		1.70		
		PVBAT=3.6V, THD=1%		1.10		

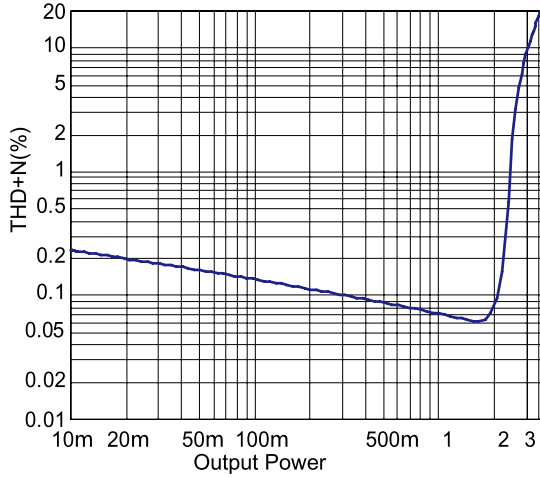
Typical Characteristics ($T_A = 25^\circ\text{C}$, $R_L = 4\Omega + 33\mu\text{H}$, NCN OFF, D MODE)



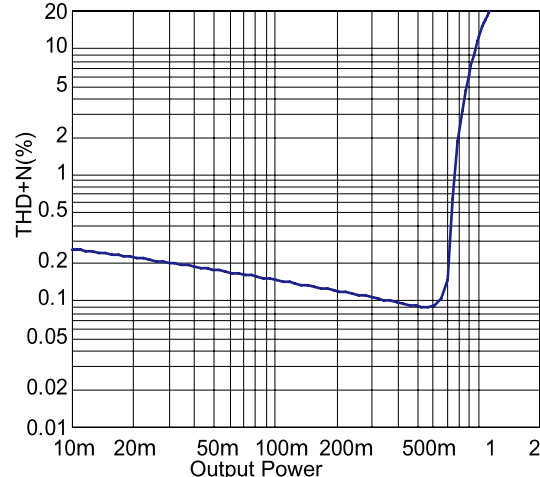
Typical Characteristics (TA=25°C, RL=4Ω+33μH, NCN OFF, D MODE)



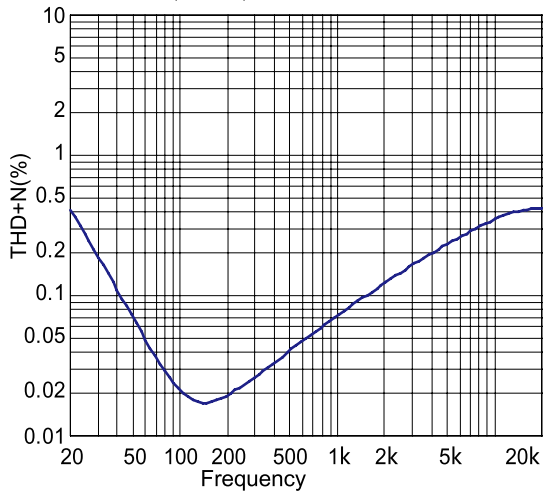
Typical Characteristics ($T_A = 25^\circ\text{C}$, $R_L = 4\Omega$, AB MODE, Charge Pump off)



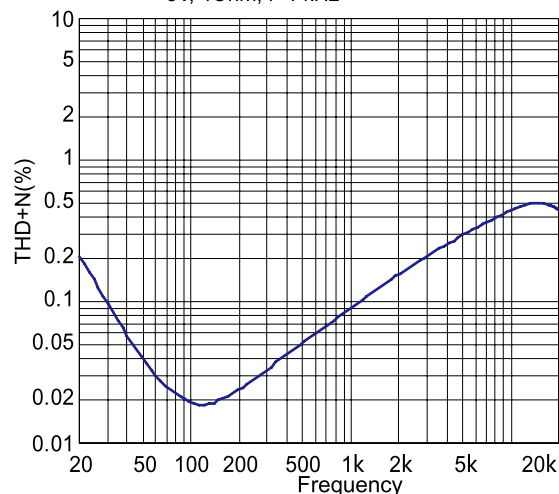
THD+N vs. Output Power
 5V, 4Ohm, f=1 kHz



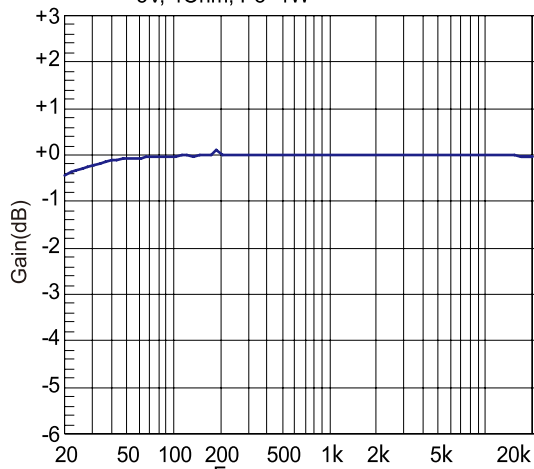
THD+N vs. Output Power
 3V, 4Ohm, f=1 kHz



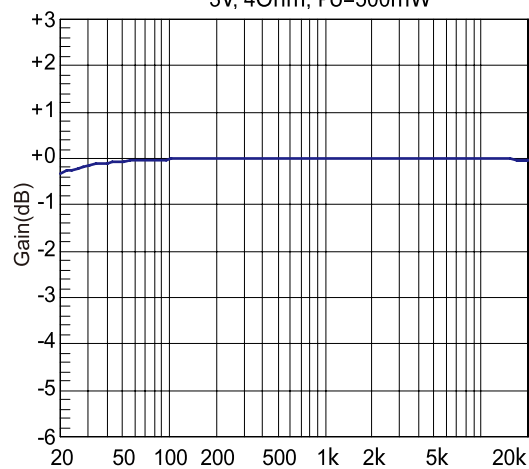
THD+N vs. Frequency
 5V, 4Ohm, $P_o = 1\text{W}$



THD+N vs. Frequency
 3V, 4Ohm, $P_o = 500\text{mW}$



Frequency Response
 5V, 4Ohm

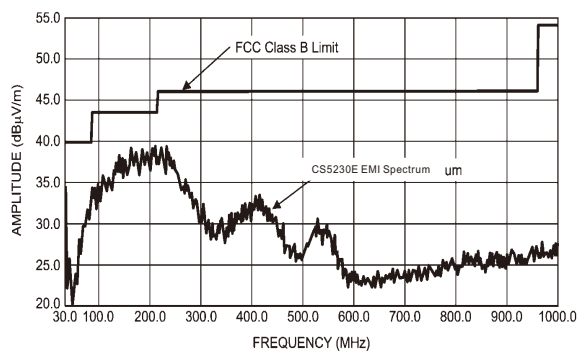


Frequency Response
 3V, 4Ohm

Product Features

CS5230E has built-in charge pump boost module, which can be used for 4Ω It provides up to 5.2W continuous power in the voltage range of lithium battery, and integrates class AB and class D audio amplifiers.

CS5230E adopts the proprietary AERC (adaptive edge rate control) technology, which greatly reduces the EMI interference in the full audio bandwidth. For the 60cm audio line, it has a margin of more than 20dB under the FCC standard (as shown in the figure below).



The PWM modulation structure without filter reduces the number of external components, PCB area and system cost, and simplifies the design. The chip has built-in overcurrent protection, overheat protection and undervoltage protection functions, which ensure that the chip is turned off under abnormal working conditions, effectively protecting the chip from damage. When the abnormal conditions are eliminated, CS5230E has the self recovery function to make the chip work again.

No Filter Required

CS5230E adopts PWM modulation without filter, which saves LC filter of traditional class D amplifier and improves efficiency. It provides a smaller area and lower cost implementation scheme for audio subsystem of portable devices.

Pop&Click Suppression

CS5230E has built-in special timing control circuit to achieve comprehensive pop&click suppression, which can effectively eliminate the transient noise that may appear when the system is powered on, down, wake up and shut down.

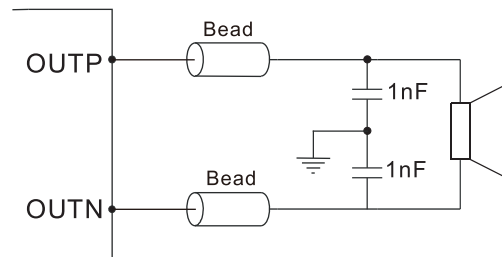
Protection Circuit

During the application of CS5230E, when the chip has a short circuit between the output pin and the power or ground, or a short circuit fault between the outputs, the overcurrent protection circuit will turn off the chip to prevent the chip from being

damaged. After the short circuit fault is eliminated, CS5230E automatically resumes operation. When the chip temperature is too high, the chip will be turned off. After the temperature drops, it can continue to work normally. When the power supply voltage is too low, the chip will also be turned off. After the power supply voltage is restored, the chip will start again.

Magnetic Beads and Capacitors

CS5230E can still meet the requirements of FCC standard for 60cm audio line without magnetic bead and capacitance. When the output audio line is too long or the device layout is close to EMI sensitive equipment, it is recommended to use magnetic beads and capacitors. Magnetic beads and capacitors should be placed as close to CS5230E as possible, as shown in the figure below.



Input Resistance (Rin)

The input of CS5230E is a differential amplifier structure, which can adopt single ended input connection method and differential input connection method. The setting of amplification factor of the two connection methods is the same. The CS5230E integrates 20KΩ Input resistance, feedback resistance is 560KΩ, Therefore, CS5230E has a fixed 28 times gain, and the amplification factor can be adjusted less than 28 times by changing the resistance of the external input resistor. The formula is as follows:

$$\text{Gain} = \frac{560\text{k}\Omega}{R_{in}+20\text{k}\Omega} \left(\frac{V}{V} \right)$$

R_{in}: input resistance of external regulation

The good matching between the two input resistors is helpful to improve the performance of PSRR, CMRR and THD, so the resistor with accuracy of 1% is required. In PCB layout, the electronics should be placed close to CS5230E to prevent the introduction of noise from high resistance nodes.

Input Capacitance (C_{in})

A high pass filter is formed between the input resistor and the input capacitor, and its cut-off frequency is as follows:

$$f_{c(-3dB)} = \frac{1}{2\pi \cdot (R_{in}+20K) \cdot C_{in}}$$

In the application, the smaller C_{in} capacitor is helpful to filter the 217Hz noise from the input, and the smaller capacitor is helpful to reduce the crackle and click when the power amplifier is turned on. Good matching between the two input capacitors is beneficial to improve the overall performance of the chip and suppress the crackle and click noise. It is recommended to use a capacitor with a tolerance of 10% or better.

Charge Pump Flying Capacitor (C_f)

Flying capacitor is used to transfer energy between power supply and charge pump load. The value of flying capacitor directly affects the load regulation rate and output driving ability of charge pump. If the flying capacitor is too small, it will affect the load adjustment rate and output driving ability of the charge pump, thus affecting the output power of the power amplifier. The larger the flying capacitor is, the stronger the load adjustment ability is, and the stronger the driving ability is. It is recommended to use X7R and X5R ceramic capacitors with voltage above 16V, 4.7uF and low ESR.

Charge Pump Holding Capacity (C_{out})

The holding capacitance and ESR of the charge pump directly affect the ripple of the output voltage of the charge pump, thus affecting the performance of the power amplifier. Recommended 470uF Above, low ESR electrolytic capacitor. As the output voltage of the charge pump is 6.2V, the holding capacitor needs to be 10V.

Power supply decoupling capacitor (C_s)

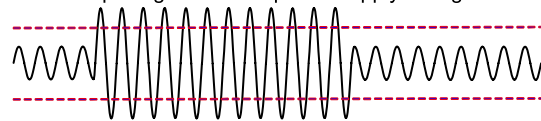
Good decoupling capacitor can improve the efficiency and performance of power amplifier. It is recommended to use X7R or X5R ceramic capacitor with low ESR. In the application of CS5230E, there are two VBAT pins, PIN1 and PIN5, where PIN1 is the power supply pin and PIN5 is the analog power supply pin. Place a 1uF ceramic capacitor on PIN5 pin to filter out high-frequency interference on the power supply. This capacitor should be placed close to PIN5 pin as much as possible;

In the application of CS5230E, PIN1 is the power supply pin, which mainly provides current for the internal charge pump circuit. This capacitor is similar to the charge reservoir, which can provide current faster than the battery, so it helps to stabilize the power supply voltage and prevent the rapid fluctuation of voltage. Here, it is recommended to use 470uF capacitor. In addition, in order to filter out lower frequency noise interference and better stabilize the analog power supply voltage, another 1uF and 10uF low ESR capacitor can be placed, And place it as close to PIN1 pin as possible.

NCN function

In audio applications, the input signal is too large or the battery voltage drops and other factors will lead to the output signal of audio power amplifier broken sound distortion, and the overload signal will cause permanent damage to the speaker. CS5230E's unique NCN function can detect the distortion of the amplifier's output signal and automatically adjust the system gain to keep the output audio signal smooth. It not only effectively avoids the damage of high-power overload output to the speaker, but also brings more comfortable hearing enjoyment.

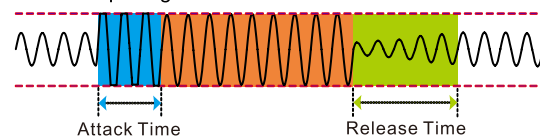
Audio output signal without power supply voltage limitation



Audio output signal in NCNOFF mode



Audio output signal in NCN mode



NCN Function Diagram

Adaptive Charge Pump Function

CS5230E internally integrates an adaptive charge pump boost circuit. When the audio signal is played, the signal size and amplitude are constantly changing. When the audio signal input is small, the output voltage amplitude is very low, and the output will not produce distortion under the normal lithium battery voltage. At this time, there is no need for a boost circuit.

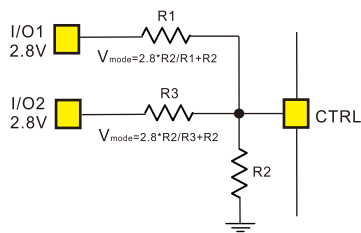
CS5230E works in pure class D mode in this case, and the conversion efficiency is about 90%; When the audio signal input is large, CS5230E automatically switches to the charge pump boost mode, which greatly reduces the power loss. The conversion efficiency of the charge pump will be limited by the output voltage, and the conversion efficiency is about equal to $V_{out}/2V_{in}$. When the power supply voltage is constant, the higher the V_{out} , the higher the conversion efficiency of the charge pump. CS5230E adopts special high-voltage process to boost CPOUT to 6.2V, and the output power can reach 5.0W.

CTRL Pin Setting

By setting the input level of the CTRL pin, you can enter various working modes of CS5230E, as shown in the table below:

CTRL Status	PA Status
0~0.3V	Shutdown
1.2~1.6V	Class AB model
1.7V~2.1V	Class D NCN ON
>2.3V	Class D NCN OFF

Based on the control mode in the above table, the following settings can be made according to the system in actual use:



If the IO control voltage of the main control is 2.8V, as shown in the figure, the switching of various working states is realized with the help of two IO ports and voltage dividing lines. When IO1 and IO2 are low, CS5230E enters the shutdown mode; When IO1 is high, IO2 is suspended. As long as the appropriate resistance ratio of R1 and R2 is selected to make the Vctrl voltage between 1.2~1.6V, CS5230E enters class AB mode; When Vctrl voltage is between 1.7~2.1V, CS5230E enters class D anti breaking mode; When IO1 is suspended and IO2 is high level, as long as the appropriate resistance ratio of R3 and R2 is selected to make the Vctrl voltage greater than 2.3V, CS5230E enters class D non anti breaking mode; The absolute values of R1 and R2 are determined by acceptable power consumption, and mode itself does not need driving current.

PCB design considerations

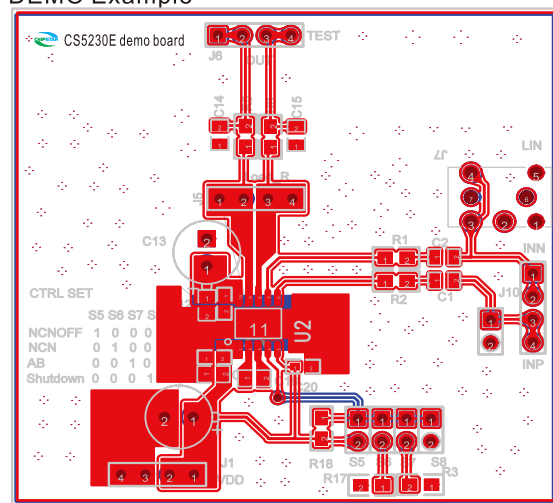
In order to give full play to the performance of CS5230E, the layout and wiring of PCB must be carefully considered

- 1: Try to walk a short and thick power line to CS5230E alone. It is recommended that the width of copper wire is greater than 1 mm. The decoupling capacitor should be placed as close to the power supply pin as possible.
- 2: The flying capacitor should be placed close to CN and CP pins of CS5230E as far as possible, the output capacitor Cout should be placed close to CPOUT pin, and the connection between capacitor and chip pin should be as short and thick as possible.
- 3: The input capacitance and resistance of CS5230E should be placed as close as possible to the INN and INP pins of the chip, and the input lines should be parallel to suppress noise coupling.

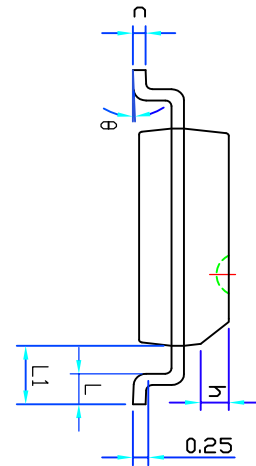
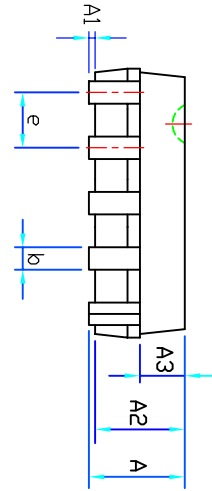
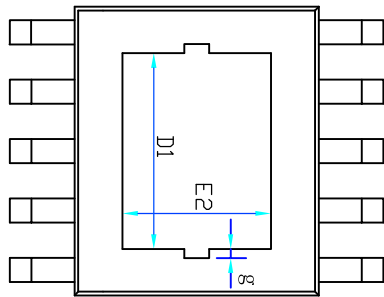
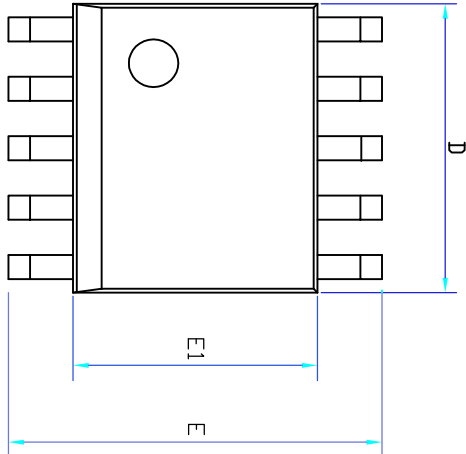
4: The magnetic beads and capacitors should be placed close to the OUTN and OUTP pins of the chip. The output line from the chip to the horn should be as short and thick as possible. The recommended copper wire width is 0.5mm.

5: In order to obtain good heat dissipation performance, the heat sink and GND pin of CS5230E should be directly connected to the large area of the layer, and the heat sink should be connected to the middle layer through the through hole.

DEMO Example



Package Information:CS5230E ESOP10L



SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	—	—	1.50
A1	0.02	0.05	0.08
A2	1.30	1.40	1.50
A3	0.70	0.75	0.80
b	0.35	—	0.45
c	0.20	—	0.24
D	4.80	4.90	5.00
D1	3.10REF		
e	1.00BSC		
E	6.05	6.15	6.25
E1	3.82	3.92	4.02
E2	2.20REF		
L	0.50	—	0.70
L1	1.15REF		
h	0.30	0.40	0.50
θ	0	—	8°
g	0.15REF		