

130mW, Differential Input DirectDrive Headphone Amplifiers

General Description

The CS4420C stereo headphone driver is designed for portable equipment where board space is at a premium. The CS4420C uses a unique DirectDrive architecture to produce a ground-referenced output from a single supply, eliminating the need for large DC-locking capacitors, saving cost, board space, and component height. The CS4420C delivers up to 130mW per channel into a 16Ω load and has low 0.006% THD + N. A high powersupply rejection ratio 86dB at 1kHz) allows this device to operate from noisy digital supplies without an additional linear regulator. Comprehensive clickand-pop circuitry suppresses audible clicks and pops on startup and shutdown. Independent left/right, low-power shutdown controls make it possible to optimize power savings in mixed mode, mono/stereo applications.

The CS4420C operates from a single 1.8V to 5.5V supply, consumes only 5mA of supply current, has short-circuit and thermal overload protection, and is specified over the extended -40°C.

CS4420C is available in a tiny 14-pin TSSOP package.

Package

- TSSOP14

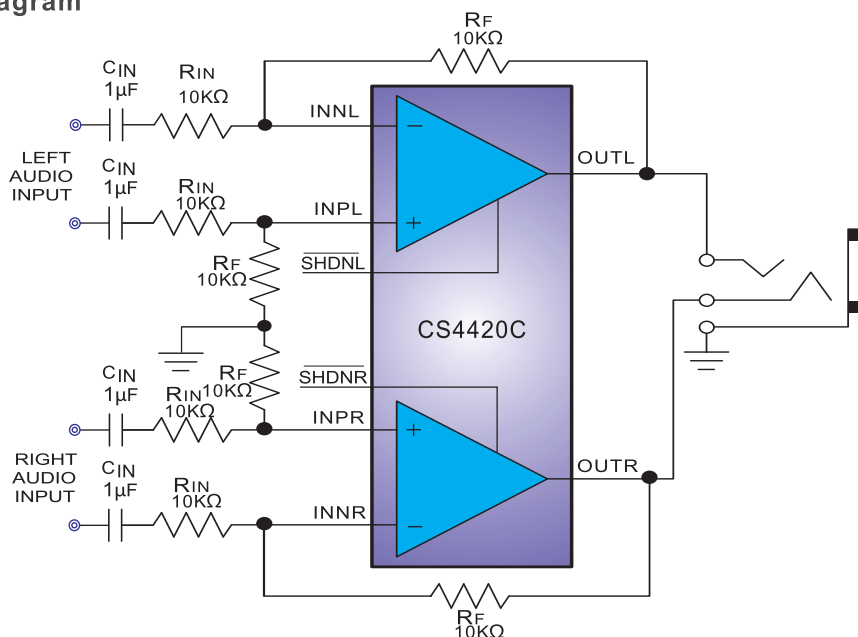
Features

- No Bulky DC-Blocking Capacitors Required
- Ground-Referenced Outputs Eliminate DC-Bias Voltages on Headphone Ground Pin
- No Degradation of Low-Frequency Response Due to Output Capacitors
- 130mW Per Channel into 16Ω
- Low 0.006% THD + N
- High PSRR (86dB at 1kHz)
- Integrated Click-and-Pop Suppression
- 1.8V to 5.5V Single-Supply Operation
- Low Quiescent Current
- Independent Left/Right, Low-Power Shutdown Controls
- Short-Circuit and Thermal Overload Protection

Applications

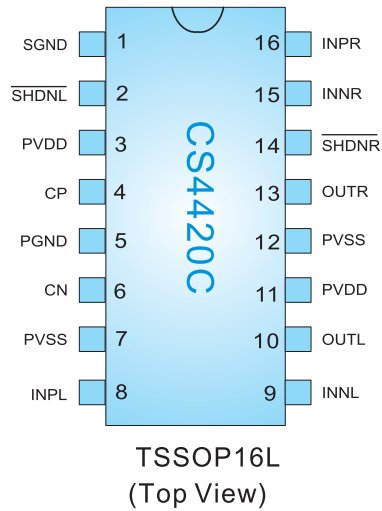
- Notebooks
- Cellular Phones
- PDAs
- MP3 Players
- Web Pads
- Portable Audio Equipment

Functional Diagram



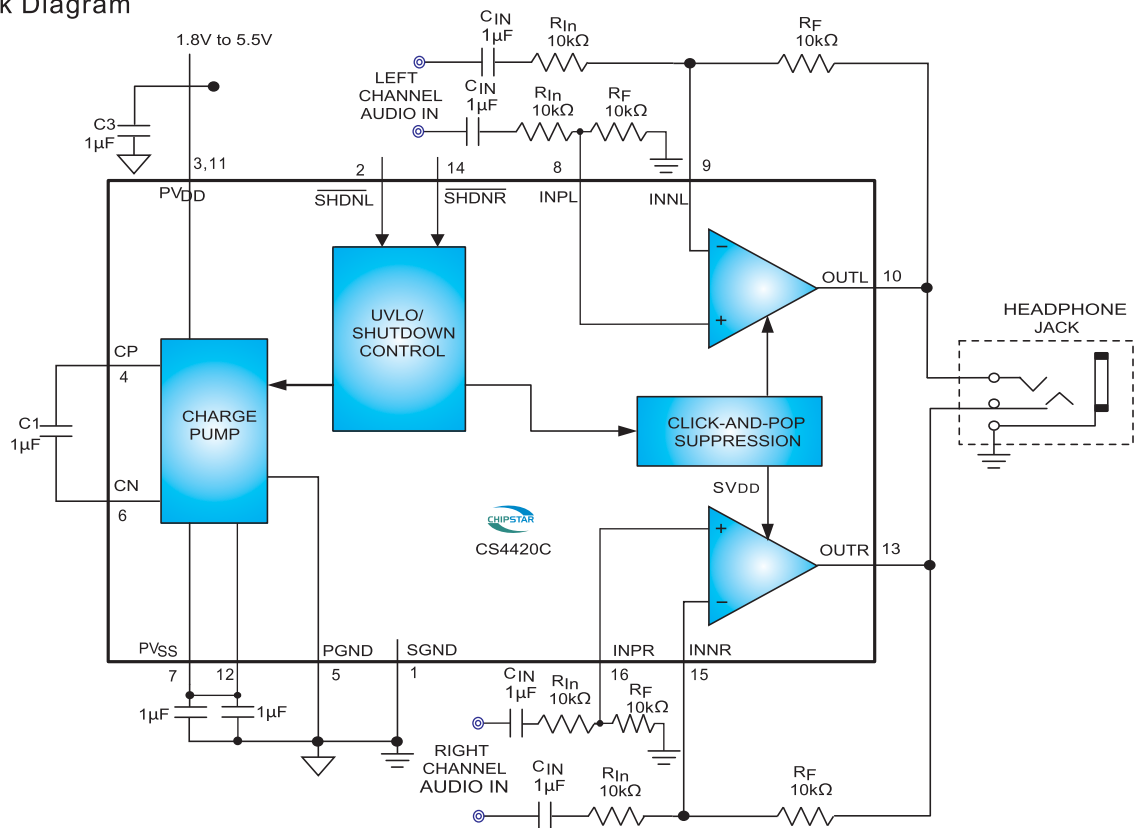
CS4420C Typical Application Circuit

Pin Description

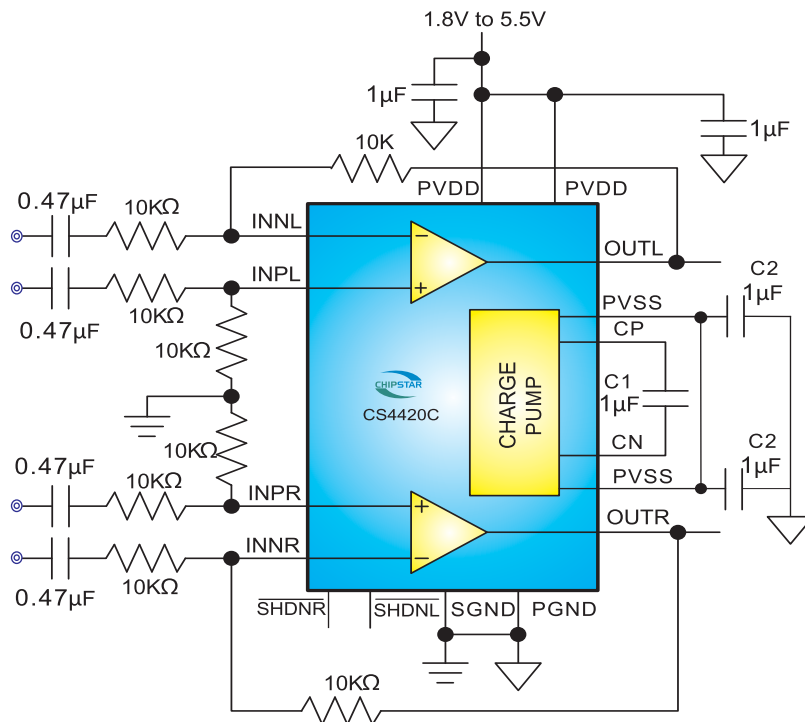


Pin No.	NAME	I/O	Function
1	SGND	GND	Signal Ground. Connect to PGND.
2	SHDNL	I	Active-Low, Left-Channel Shutdown. Connect to VDD for normal operation.
3	PVDD	P	Charge-Pump Power Supply.
4	CP	—	Flying Capacitor Positive Terminal
5	PGND	GND	Power Ground. Connect to SGND.
6	CN	—	Flying Capacitor Negative Terminal
7	PVSS	P	Charge-Pump Negative Supply Output
8	INPL	I	Positive audio Input for Left-Channel Audio
9	INNPL	I	Negative audio Input for Left-Channel Audio
10	OUTL	O	Left-Channel Output
11	PVDD	P	Charge-Pump Power Supply.
12	PVSS	P	Charge-Pump Negative Supply Output
13	OUTR	O	Right-Channel Output
14	SHDNR	I	Active-Low, Right-Channel Shutdown. Connect to VDD for normal operation.
15	INNRR	I	Negative audio Input for Right-Channel Audio
16	INPR	I	Positive audio Input for Right-Channel Audio

Block Diagram



Typical Application



Absolute Maximum Ratings ¹

Symbol	Description	Value	Unit
V _{DD}	Supply Voltage at no Input Signal	6	V
V _I	Input Voltage	-0.3 to VDD+0.3	V
T _J	Operating Junction Temperature Range	-40 to 150	°C
T _{SDR}	Maximum Lead Soldering Temperature , 10 Seconds	300	°C
T _{STG}	Storage Temperature Range	-65 to 150	°C

Recommended Operating Conditions

Symbol	Description	Value	Unit
V _{DD}	Supply Voltage	1.8~5.5	V
T _A	Ambient Temperature Range	-40~85	°C
T _J	Junction Temperature Range	-40~125	°C

Thermal Information ²

Symbol	Description	Value	Unit
θ _{JA}	Thermal Resistance-Junction to Ambient	160	°C/W
θ _{JC}	Thermal Resistance-Junction to Case	56	°C/W

Ordering and Marking Information

Device	Package Type	Device Marking	Reel Size	Tape Width	Quantity
CS4420C	TSSOP16		13"	12mm	3000 units

ESD Susceptibility

ESD Susceptibility-HBM ----- ±6kV

ESD Susceptibility-MM ----- ±200V

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at one time.

ELECTRICAL CHARACTERISTICS

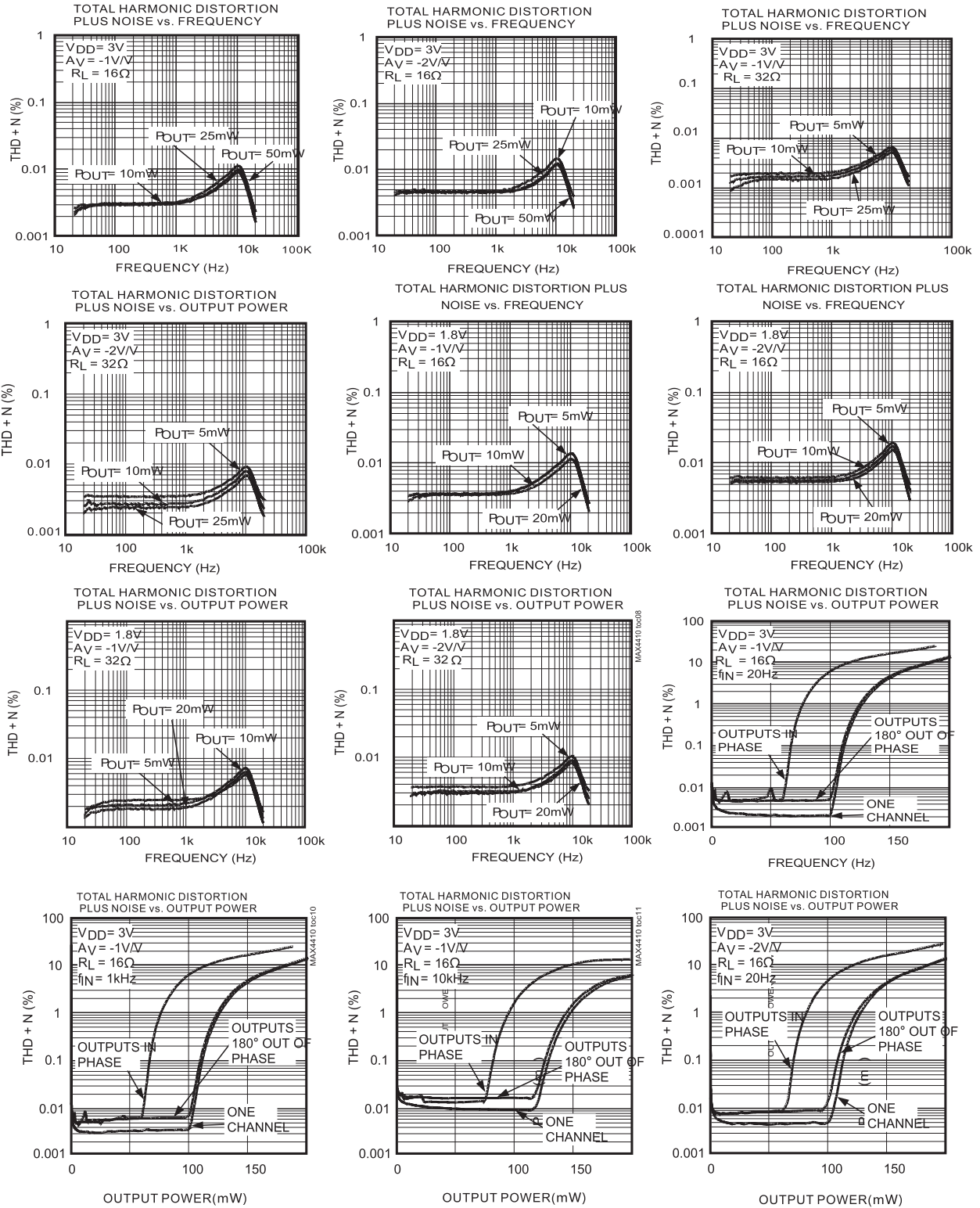
($P_{V_{DD}} = S_{V_{DD}} = 3V$, $P_{GND} = S_{GND} = 0V$, $S_{HDNL} = S_{HDNR} = S_{V_{DD}}$, $C_1 = C_2 = 1\mu F$, $C_{IN} = 1\mu F$, $R_L = \infty$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	VDD	Guaranteed by PSRR test		1.8	3.0	5.5	V
Quiescent Supply Current	IDD	One channel enabled		3.0			mA
		Two channel enabled		4.0			
Shutdown Supply Current	ISHDN	SHDNL=SHDNR=GND		1.0			µA
$\overline{\text{SHDN}}$ _ Thresholds		VIH		1.4			V
		VIL		0.4			
SHDN_Input Leakage Current				-1	+1		µA
SHDN_to Full Operation	tSON			36			ms
CHARGE PUMP							
Oscillator Frequency	fOSC			400	500	600	kHz
AMPLIFIERS							
Input Offset Voltage	VOs	Input AC-coupled, RL = 32 Ω		0.35			mV
Power-Supply Rejection Ratio	PSRR	1.8V ≤ VDD ≤5.5V	Dc	75	90		dB
		200mVP-P ripple	fRIPPLE = 1kHz	90			
			fRIPPLE = 20kHz	55			
Output Power	POUT	THD + N = 1%	RL = 32 Ω	24	90	260	mW
			RL = 16 Ω	25	97	300	
Total Harmonic Distortion Plus Noise	THD + N	fIN= 1kHz	RL = 32Ω POUT = 25mW	0.005			%
			R = 16Ω POUT = 50mW	0.01			
Signal-to-Noise Ratio	SNR	RL = 32Ω, POUT = 20mW, fIN = 1kHz		95			dB
Slew Rate	SR			0.8			V/µs
Maximum Capacitive Load	CL	No sustained oscillations		300			pF
Crosstalk		RL = 16Ω, POUT = 1.6mW, fIN = 10kHz		70			dB
Thermal Shutdown Threshold				140			°C
Thermal Shutdown Hysteresis				15			°C

Note : All specifications are 100% tested at $T_A = +25^\circ C$; temperature limits are guaranteed by design.

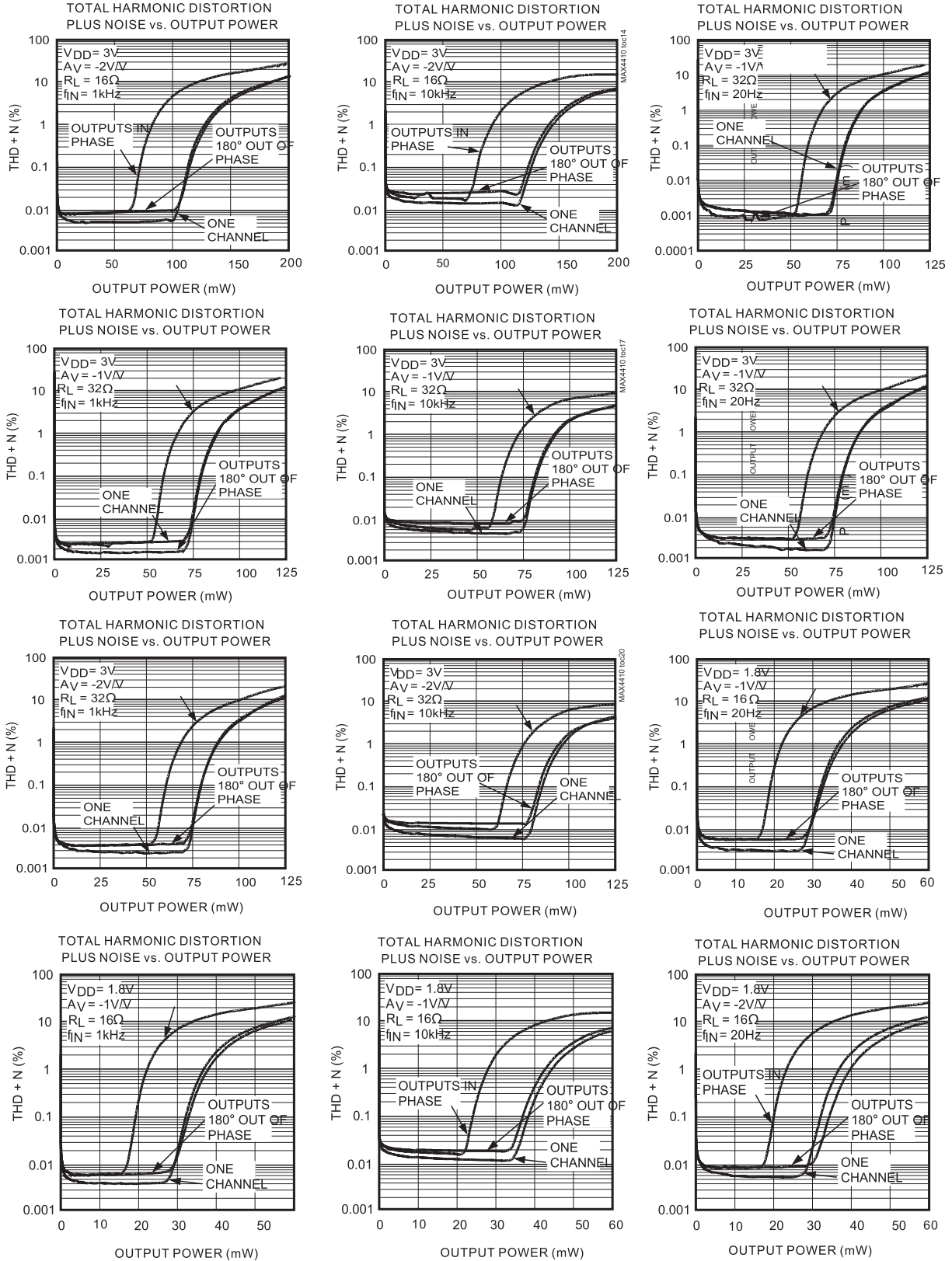
Typical Operating Characteristics

(C1 = C2 = 2.2 μ F, THD + N measurement bandwidth = 22Hz to 22kHz, TA = +25°C, unless otherwise noted.)



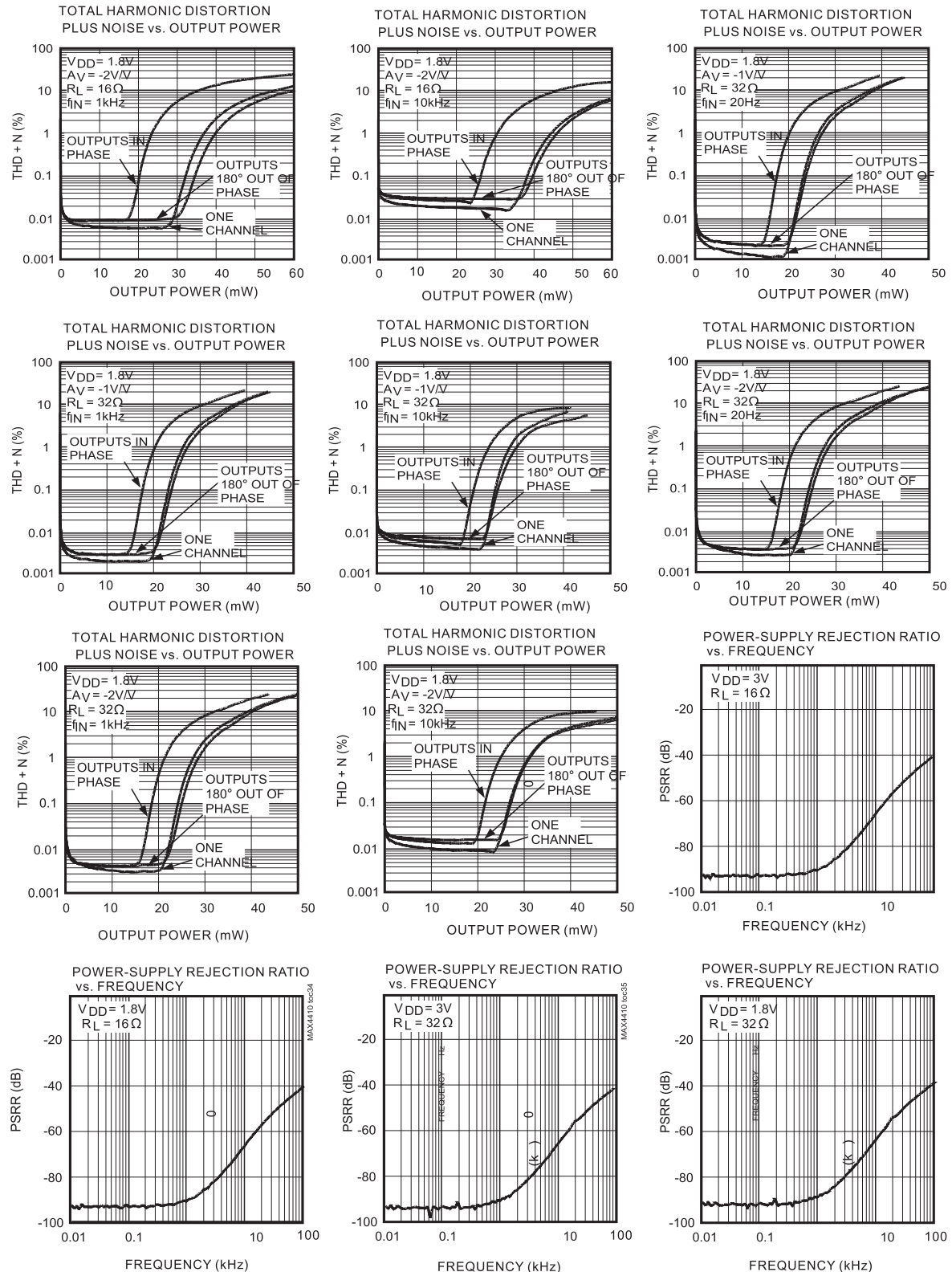
Typical Operating Characteristics

(C1 = C2 = 2.2 μ F, THD + N measurement bandwidth = 22Hz to 22kHz, TA = +25°C, unless otherwise noted.)



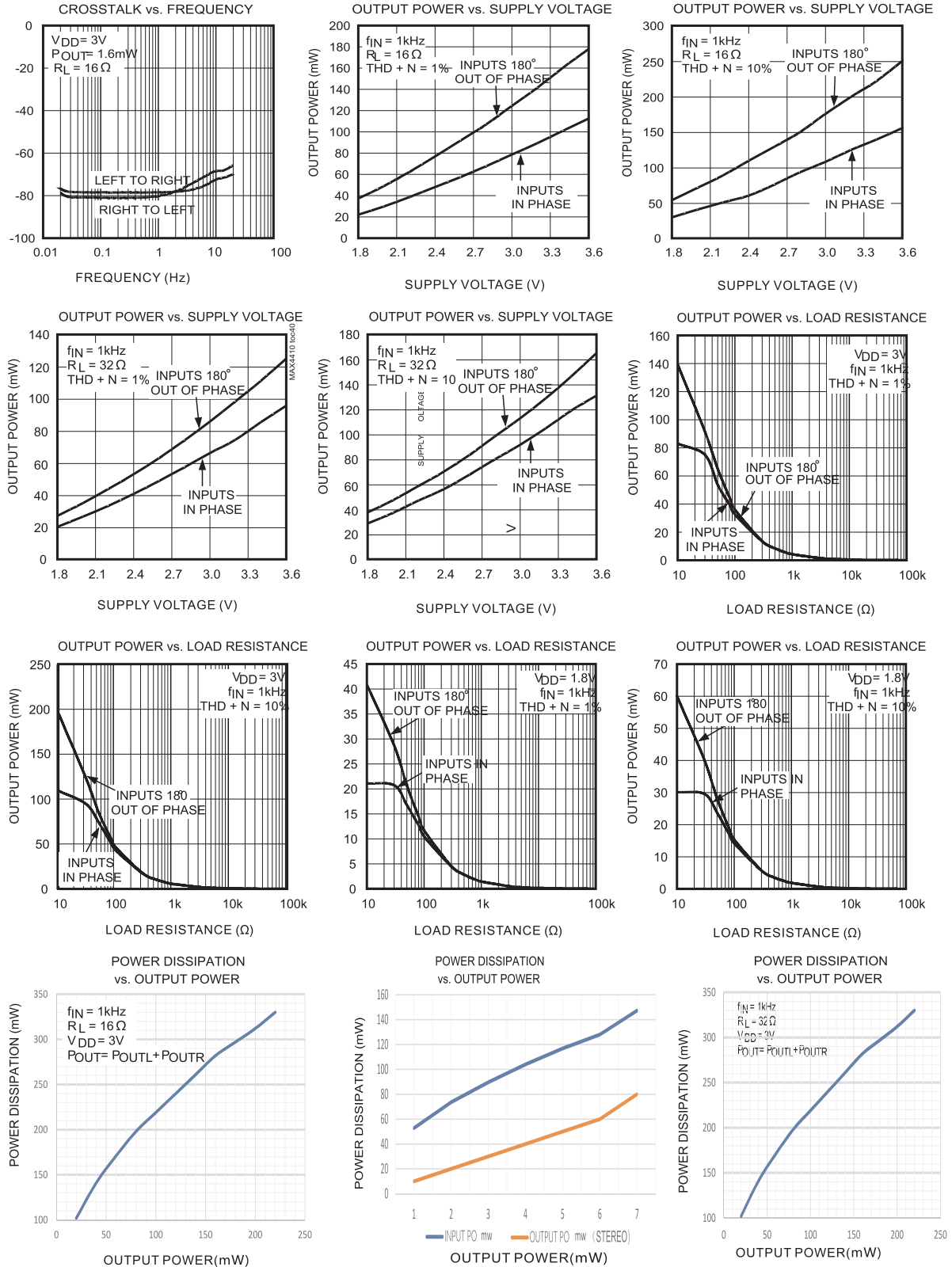
Typical Operating Characteristics

(C1 = C2 = 2.2 μ F, THD + N measurement bandwidth = 22Hz to 22kHz, TA = +25°C, unless otherwise noted.)



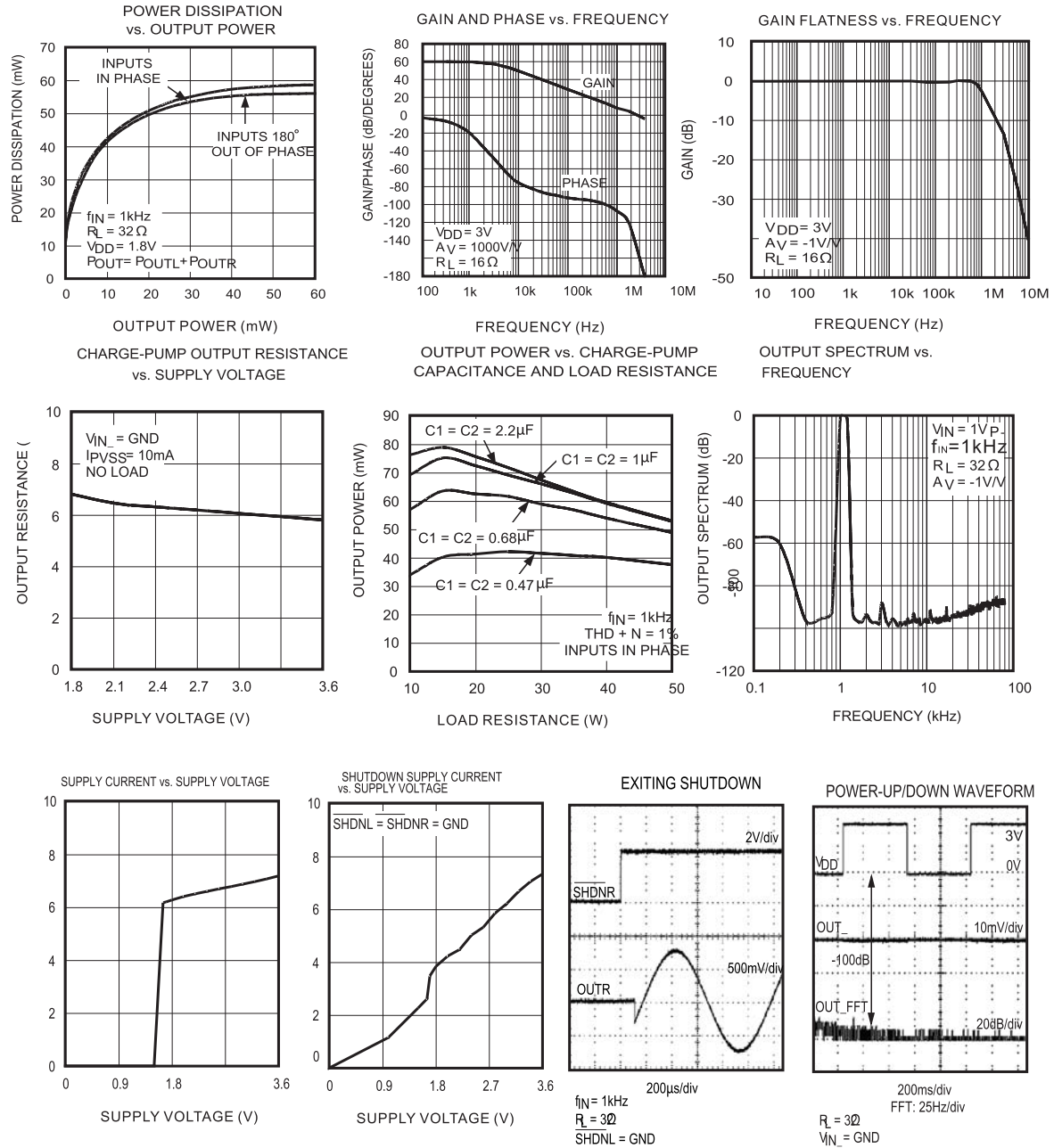
Typical Operating Characteristics

(C1 = C2 = 2.2μF, THD + N measurement bandwidth = 22Hz to 22kHz, TA = +25°C, unless otherwise noted.)



Typical Operating Characteristics

(C1 = C2 = 2.2 μ F, THD + N measurement bandwidth = 22Hz to 22kHz, TA = +25°C, unless otherwise noted.)



Detailed Description

The CS4420C stereo headphone driver features DirectDrive architecture, eliminating the large output coupling capacitors required by traditional single-supply headphone drivers. The device consists of two 130mW ClassAB headphone drivers, undervoltage lockout (UVLO)/shutdown control, charge-pump, and comprehensive click-and-pop suppression circuitry (see Typical Application Circuit). The charge pump inverts the positive supply (PVDD), creating a negative supply (PVSS). The headphone drivers operate from these bipolar supplies with their outputs biased about GND (Figure 1). The drivers have almost twice the supply range compared to other 3V single-supply drivers, increasing the available output power. The benefit of this GND bias is that the driver outputs do not have a DC component typically VDD/2. Thus, the large DC-blocking capacitors are unnecessary, improving frequency response while conserving board space and system cost.

Each channel has independent left/right, active-low shutdown controls, making it possible to optimize power savings in mixed-mode, mono/stereo operation. The device features an undervoltage lockout that prevents operation from an insufficient power supply and click-and-pop suppression that eliminates audible transients on startup and shutdown. Additionally, the CS4420C features thermal overload and short-circuit protection

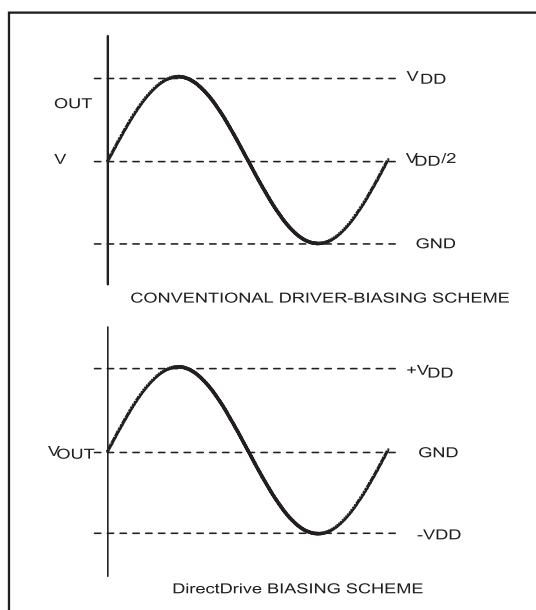


Figure 1. Traditional Driver Output Waveform vs. CS4420C Output Waveform

DirectDrive

Traditional single-supply headphone drivers have their outputs biased about a nominal DC voltage (typically half the supply) for maximum dynamic range. Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone driver. DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the outputs of the CS4420C to be biased about GND, almost doubling dynamic range while operating from a single supply. With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220μF, typ) tantalum capacitors, the CS4420C charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone driver. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the Typical Operating Characteristics for details of the possible

capacitor sizes. There is a low DC voltage on the driver outputs due to amplifier offset. However, the offset of the CS4420C is typically 0.5mV, which, when combined with a 32Ω load, results in less than 32μA of DC current flow to the headphones.

Low-Frequency Response

In addition to the cost and size disadvantages of the DC-blocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal.

1) The impedance of the headphone load and the DC-blocking capacitor form a highpass filter with the -3dB point set by:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}}$$

where R_L is the headphone impedance and C_{OUT} is the DC-blocking capacitor value. The highpass filter is required by conventional single-ended, single power-supply headphone drivers to block the midrail DC bias component of the audio signal from the headphones. The drawback to the filter is that it can attenuate low-frequency signals. Larger values of C_{OUT} reduce this effect but result in physically larger, more expensive capacitors. Figure 2 shows the relationship between the size of C_{OUT} and the resulting low-frequency attenuation. Note that the -3dB point for a 16Ω headphone with a 100μF blocking capacitor is 100Hz, well within the normal audio band, resulting in low-frequency attenuation of the reproduced signal.

2) The voltage coefficient of the DC-blocking capacitor contributes distortion to the reproduced audio signal as the capacitance value varies as a function of the voltage change across the capacitor. At low frequencies, the reactance of the capacitor dominates at frequencies below the -3dB point and the voltage coefficient appears as frequency-dependent distortion. Figure 3 shows the THD + N introduced by two different capacitor dielectric types. Note that below 100Hz, THD + N increases rapidly. The combination of low-frequency attenuation and frequency-dependent distortion compromises audio reproduction in portable audio equipment that emphasizes low-frequency effects such as multimedia laptops, as well as MP3, CD, and DVD players. By eliminating the DC-blocking capacitors through DirectDrive technology, these capacitor-related deficiencies are eliminated. The CS4420C features a low-noise charge pump. The 320kHz switching frequency is well beyond the audio range, and thus does not interfere with the audio signals. The switch drivers feature a controlled switching

speed that minimizes noise generated by turn-on and turn-off transients. By limiting the switching speed of the switches, the di/dt noise caused by the parasitic bond wire and trace inductance is minimized. Although not typically required, additional high-frequency noise attenuation can be achieved by increasing the size of C_2 (see Typical Application Circuit).

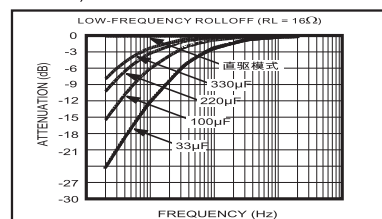


Figure 2. Low-Frequency Attenuation for Common DC-Blocking Capacitor Values

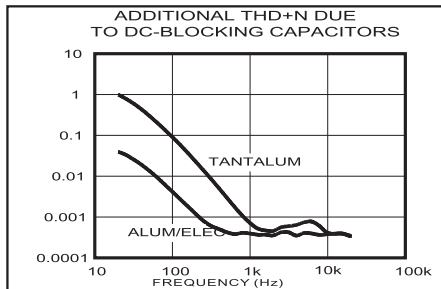


Figure 3. Distortion Contributed by DC-Blocking Capacitors

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range, select capacitors with an X7R dielectric.

Shutdown

The CS4420C features two shutdown controls allowing either channel to be shut down or muted independently. $\overline{\text{SHDNL}}$ controls the left channel while $\overline{\text{SHDNR}}$ controls the right channel. Driving either $\overline{\text{SHDN}}$ low disables the respective channel, sets the driver output impedance to about 1kΩ, and reduces the supply current to less than 10μA. When both $\overline{\text{SHDN}}$ inputs are driven low, the charge pump is also disabled, further reducing supply current draw to 6μA. The charge pump is enabled once either $\overline{\text{SHDN}}$ input is driven high.

Power Dissipation

Under normal operating conditions, linear power amplifiers can dissipate a significant amount of power. The maximum power dissipation for each package is given in the Absolute Maximum Ratings section under Continuous Power Dissipation or can be calculated by the following equation:

$$P_{\text{DISSIPG(MAX)}} = \frac{T_J(\text{MAX}) - T_A}{\theta_{JA}}$$

where $T_J(\text{MAX})$ is +150°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in °C/W as specified in the Absolute Maximum Ratings section. For example, θ_{JA} of the TSSOP package is +109.9°C/W.

The CS4420C has two sources of power dissipation, the charge pump and the two drivers. If the power dissipation for a given application exceeds the maximum allowed for a given package, either reduce VDD, increase load impedance, decrease the ambient temperature, or add heat sinking to the device. Large output, supply, and ground traces improve the maximum power dissipation in the package. Thermal overload protection limits total power dissipation in the CS4420C. When the junction temperature exceeds +140°C, the thermal protection circuitry disables the amplifier output stage. The amplifiers are enabled once the junction temperature cools by 15°C. This results in a pulsing output under continuous thermal overload conditions.

Output Power

The device has been specified for the worst-case scenario—when both inputs are in phase. Under this condition, the drivers simultaneously draw current from the charge pump, leading to a slight loss in headroom of VSS. In typical stereo audio applications, the left and right signals have differences in both magnitude and phase, subsequently leading to an increase in the maximum attainable output power.

Powering Other Circuits from a Negative Supply

An additional benefit of the CS4420C is the internally generated, negative supply voltage (-VDD). This voltage is used by the CS4420C to provide the ground-referenced output level. It can, however, also be used to power other devices within a design. Current draw from this negative supply (PVSS) should be limited to 5mA, exceeding this will affect the operation of the headphone driver. The negative supply voltage appears on the PVSS pin. A typical application is a negative supply to adjust the contrast of LCD modules. When considering the use of PVSS in this manner, note that the charge-pump voltage at PVSS is roughly proportional to -VDD and is not a regulated voltage. The charge-pump output impedance plot appears in the Typical Operating Characteristics.

Compensation Capacitor

The stability of the CS4420C is affected by the value of the feedback resistor (RF). The combination of RF and the input and parasitic trace capacitance introduces an additional pole. Adding a capacitor in parallel with RF compensates for this pole. Under typical conditions with proper layout, the device is stable without the additional capacitor.

Input Filtering

The input capacitor (Cin), in conjunction with RIN, forms a highpass filter that removes the DC bias from an incoming signal (see Typical Application Circuit). The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3\text{dB}} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose RIN according to the Gain-Setting Resistors section. Choose the CIN such that f-3dB is well below the lowest frequency of interest. Setting f-3dB too high affects the low-frequency response of the amplifier. Use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies. Other considerations when designing the input filter include the constraints of the overall system and the actual frequency band of interest. Although high-fidelity audio calls for a flat-gain response between 20Hz and 20kHz, portable voice-reproduction devices such as cellular phones and two-way radios need only concentrate on the frequency range of the spoken human voice (typically 300Hz to 3.5kHz). In addition, speakers used in portable devices typically have a poor response below 150Hz. Taking these two factors into consideration, the input filter may not need to be designed for a 20Hz to 20kHz response, saving both board space and cost due to the use of smaller capacitors.

Flying Capacitor (C1)

The value of the flying capacitor (C1) affects the load regulation and output resistance of the charge pump. A C1 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C1 improves load regulation and reduces the charge-pump output resistance to an extent. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the Typical Operating Characteristics. Above 2.2μF, the on-resistance of the switches and the ESR of C1 and C2 dominate.

Output Capacitor (C2)

The output capacitor value and ESR directly affect the ripple at PVSS. Increasing the value of C2 reduces output ripple. Likewise, decreasing the ESR of C2 reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the Typical Operating Characteristics.

Power-Supply Bypass Capacitor

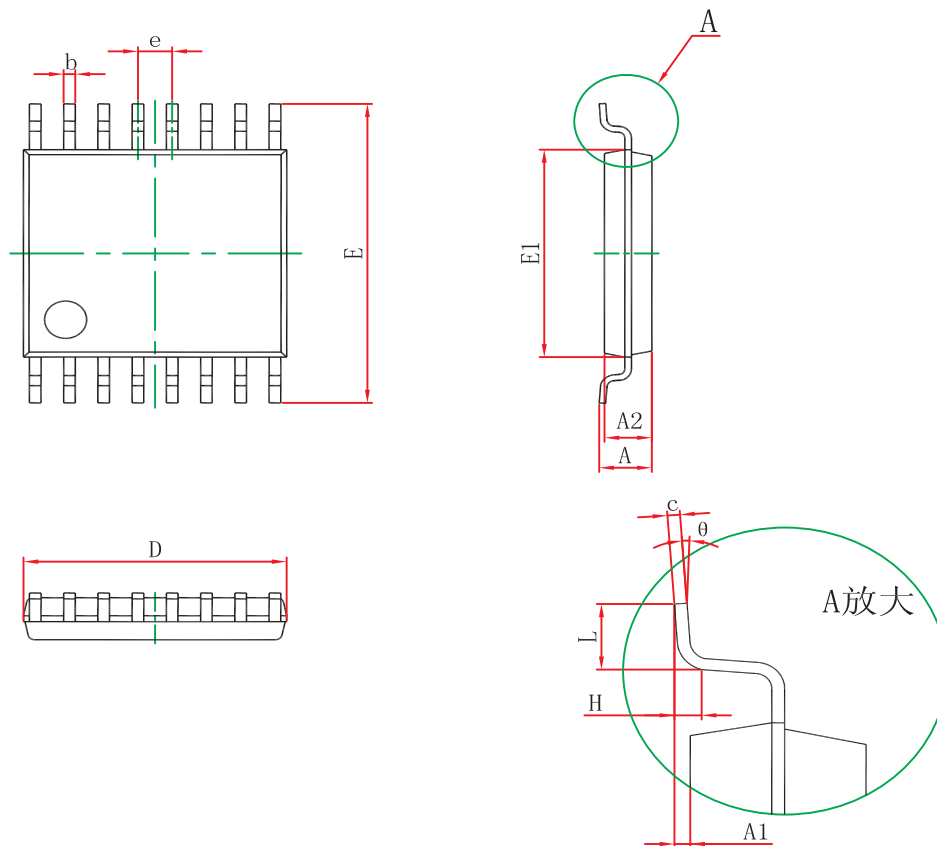
The power-supply bypass capacitor (C3) lowers the output impedance of the power supply, and reduces the impact of the CS4420C's charge-pump switching transients. Bypass PVDD with C3, the same value as C1, and place it physically close to the PVDD and PGND pins.

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Connect PGND and SGND together at a single point on the PC board. Connect all components associated with the charge pump (C2 and C3) to the PGND plane. Connect PVDD and SVDD together at the device. Connect PVSS and SVSS together at the device. Bypassing of both supplies is accomplished by charge-pump capacitors C2 and C3 (see Typical Application Circuit). Place capacitors C2 and C3 as close to the device as possible. Route PGND and all traces that carry switching transients away from SGND and the traces and components in the audio signal path.

Package Information

CS4420C TSSOP16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	6.250	6.550	0.246	0.258
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	4.300	4.500	0.169	0.177
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

Notes:

(1) All dimensions are in millimeters. Angles in degrees.